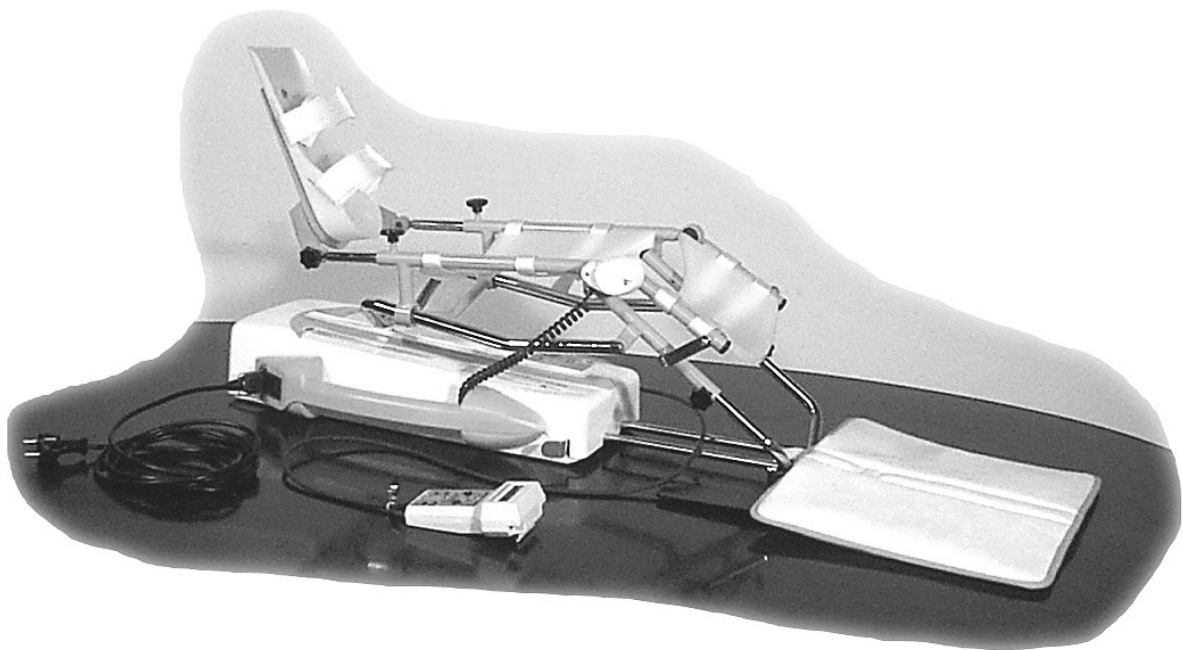


ATTELLE DE GENOU



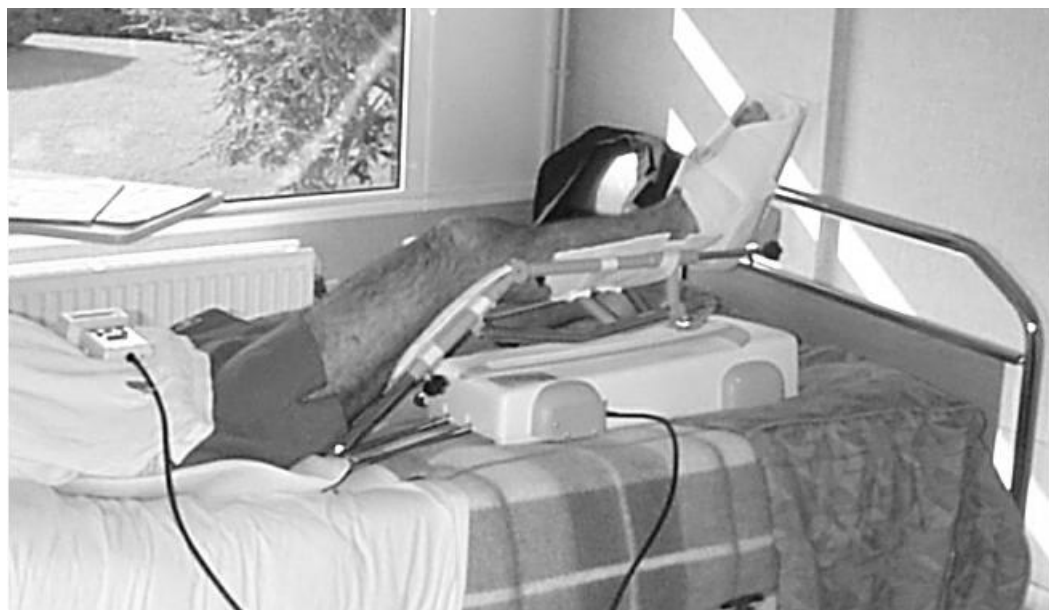
- Dossier technique -

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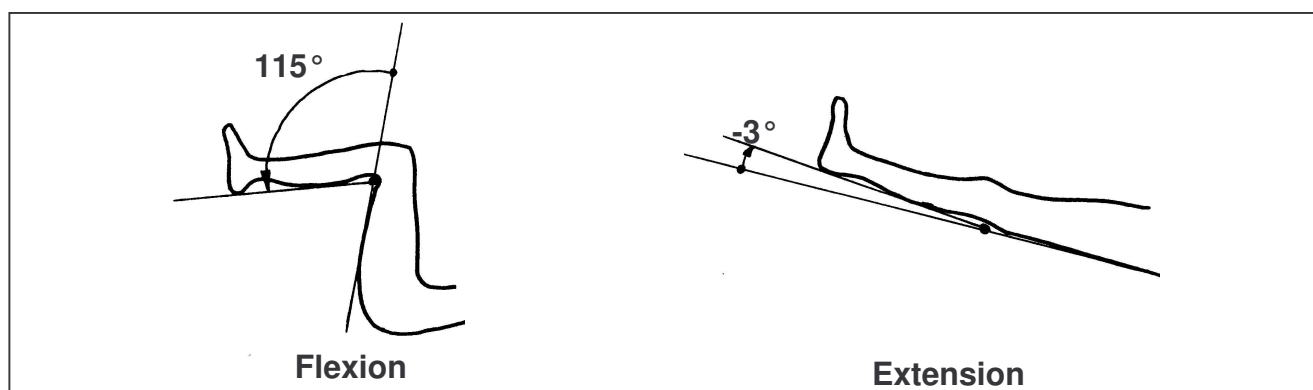
1. INTRODUCTION :

En observant son intervention sur un patient nécessitant une rééducation passive du genou ou de la hanche, un kinésithérapeute a remarqué que cette intervention était composée de gestes simples et répétitifs : l'idée était de trouver un produit capable d'automatiser cette intervention manuelle sur le patient. Le produit ainsi réalisé peut permettre une mobilisation précoce, une récupération rapide des amplitudes, une diminution de la douleur post opératoire associée à une réduction de la médication antalgique chez le patient.

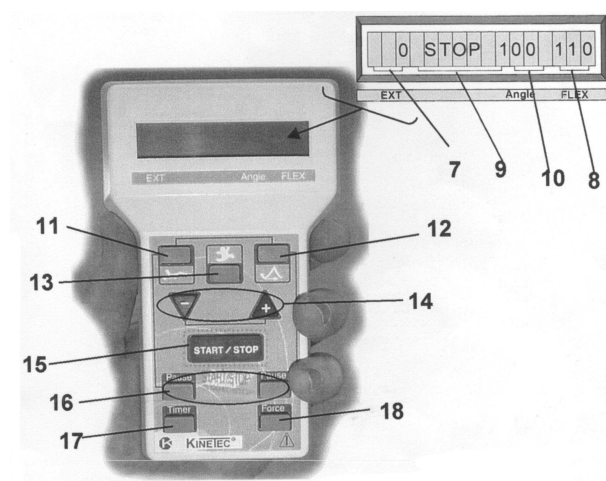


2. MISE EN SITUATION :

Le produit doit pouvoir assurer la mobilisation articulaire passive du genou (et/ou de la hanche) dans une plage angulaire de -3° à 115° .



Son utilisation est la suivante : (extrait du guide d'utilisation de l'attelle de genou **Adventa+**)



Mise en route de l'attelle : pour démarrer l'attelle il faut appuyer sur la touche **START/STOP (15)**

Réglage de la limite d'extension (-3° à 110°C) : il faut dans un premier temps sélectionner l'extension grâce au bouton poussoir (11), la valeur réglée s'affiche. On peut ensuite modifier cette valeur grâce aux boutons **plus(+)** et **moins(-)** (14).

Réglage de la limite de flexion (2° à 115°C) : il faut dans un premier temps sélectionner la flexion grâce au bouton poussoir (12), la valeur réglée s'affiche. On peut ensuite modifier cette valeur grâce aux boutons **plus(+)** et **moins(-)** (14).

Réglage de la vitesse (1 à 5) : il faut dans un premier temps sélectionner la vitesse grâce au bouton poussoir (13), la valeur réglée s'affiche. On peut ensuite modifier cette valeur grâce aux boutons **plus (+)** et **moins (-)** (14).

Arrêt du mouvement : le patient a la possibilité d'arrêter le mouvement à tout moment lorsqu'il sent une douleur. Cet arrêt se fait par la touche **START/STOP (15)**. Lorsque le patient appui de nouveau sur **START/STOP (15)** le mouvement de l'attelle est enclenché dans l'autre sens.

Affichage : l'attelle affiche en permanence les réglages limites de flexion et d'extension ainsi que sa position courante.

Remarques :

-Lorsque l'attelle arrive en limite d'extension ou de flexion, le mouvement s'arrête pendant une seconde puis repart dans l'autre sens.

-Les touches (16)(17)(18) ne sont pas utilisées dans la version à notre disposition.

Symboles utilisés :

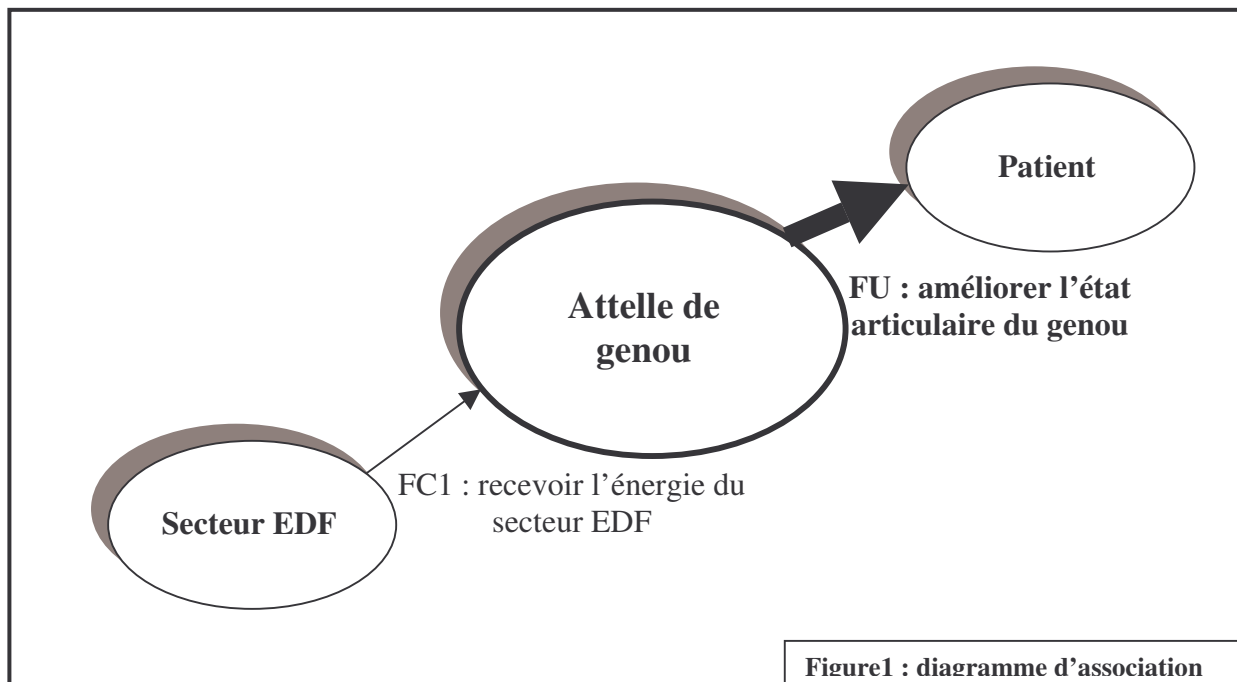
	Appareil de TYPE B (protection contre les chocs électriques)
	ATTENTION (consulter les documents d'accompagnement)
	ARRÊT (mise hors-tension)
	MARCHE (mise sous-tension)
	Platine électronique sous tension (12Vdc)

	VITESSE
	EXTENSION
	FLEXION
	Service
	Poignée de commande

3. ENVIRONNEMENT DU SYSTEME

3.1 Diagramme d'association

Dans ce diagramme, on retrouve les milieux extérieurs principaux de l'attelle de genou.



3.2 Diagramme sagittal

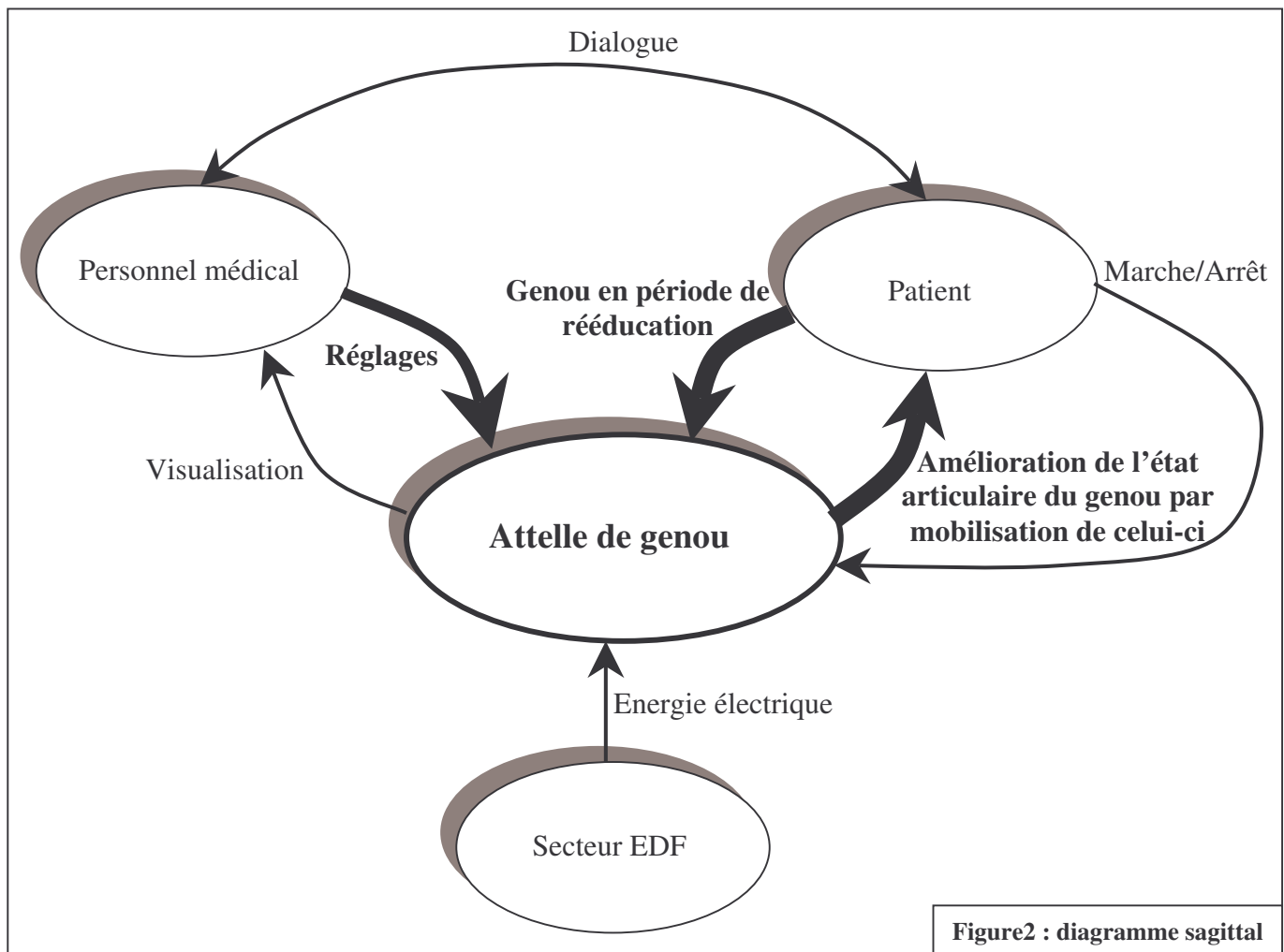


Figure2 : diagramme sagittal

Le **personnel médical** règle au préalable l'attelle de genou grâce à un clavier et à l'affichage des données sur un écran LCD. Les réglages sont les suivants :

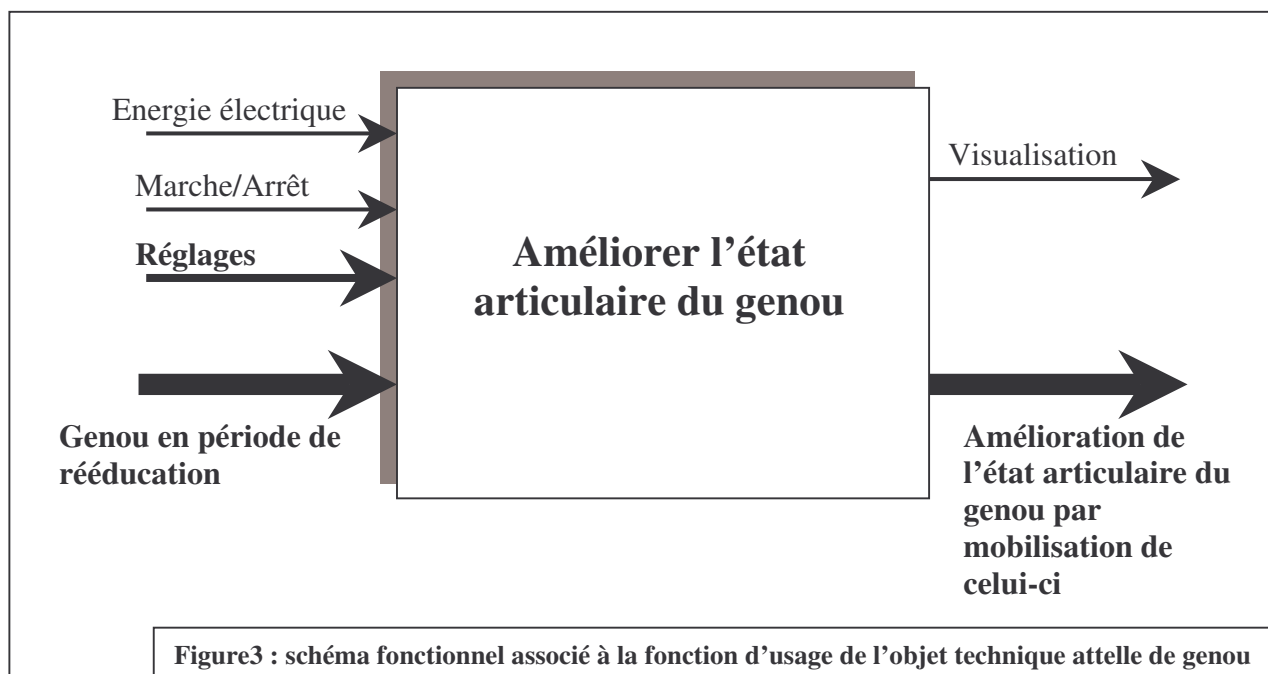
- limite d'extension (-3° , 110°),
- limite de flexion (2° , 115°),
- vitesse (1 à 5) ($50^{\circ}/\text{min}$ à $150^{\circ}/\text{min}$).

L'**attelle de genou** permet de mobiliser le genou du patient afin d'améliorer son état articulaire. Le mouvement de l'attelle alterne entre la flexion et extension. L'amplitude du mouvement dépend des réglages des limites d'extension et de flexion. Lorsque l'angle du genou arrive à une limite de flexion et d'extension alors le mouvement de l'attelle s'arrête pendant une seconde avant de changer de sens.

Le **patient** a la possibilité d'arrêter l'attelle de genou lorsqu'il ressent une douleur. Lorsque le patient appuie de nouveau sur Marche/Arrêt alors le mouvement de l'attelle est enclenché dans l'autre sens.

4. ANALYSE FONCTIONNELLE DE L'OBJET TECHNIQUE : ATTELLE DE GENOU

4.1 Fonction d'usage de l'objet technique : attelle de genou



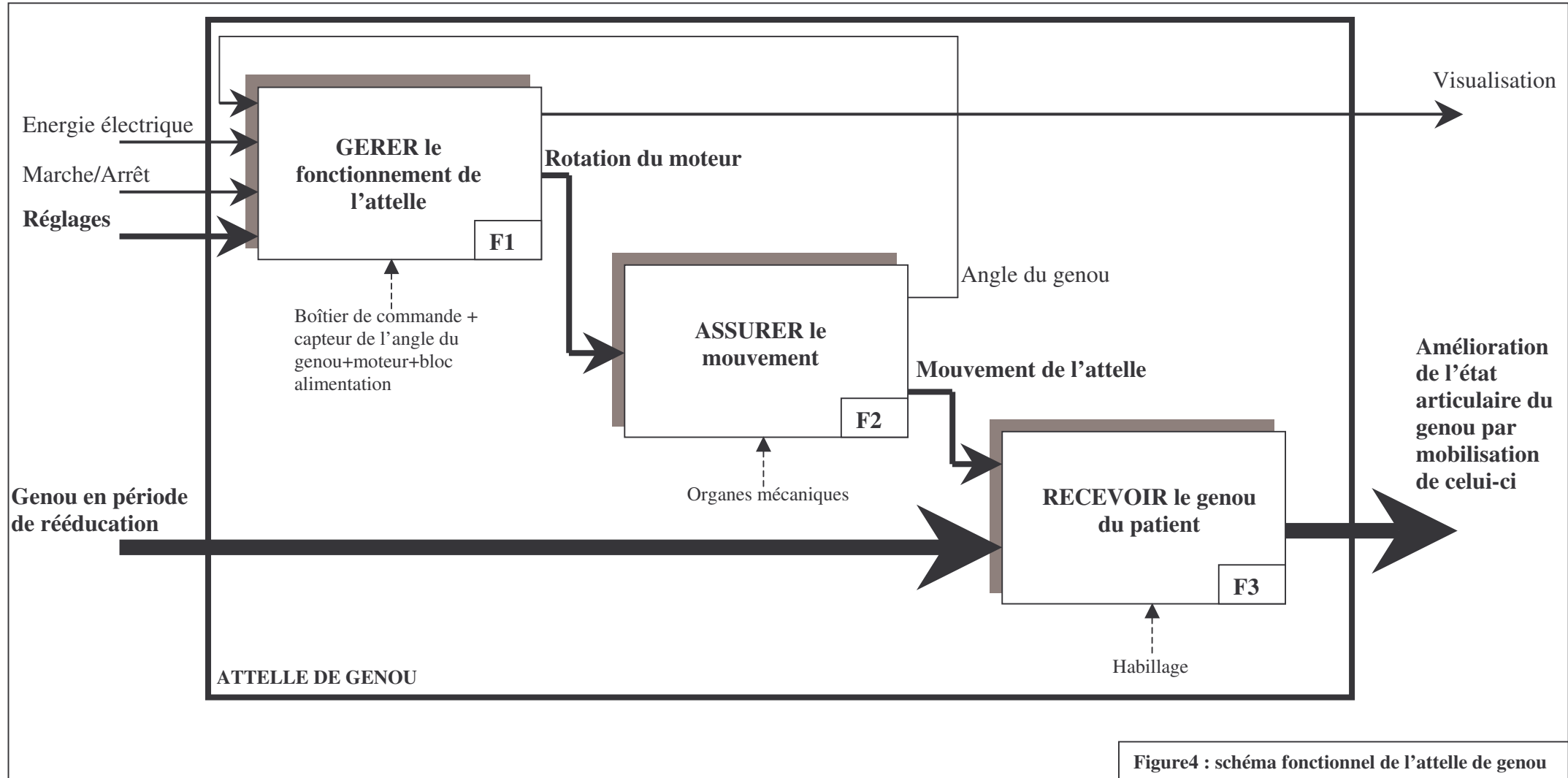
L'attelle de genou permet donc d'**améliorer** l'état articulaire du genou par mobilisation de celui-ci.

4.2 Cahier des charges de l'objet technique attelle de genou

Critères	Niveaux	Flexibilités
Amplitude genou : Flexion Extension Vitesse du cycle	de 2° à 115° de -3° à 110° 50 à 150°/min	$\pm 1^\circ$ $\pm 1^\circ/\text{min}$
Puissance absorbée	< 15 W	$1 < P \text{ (W)} < 15$
Electrique	Appareil de type B classe 1	
Physique	Le mouvement est inversé si une résistance excessive est rencontrée	
Fabrication	Norme IEC 601.1	
Commande	Instantanée	$0 < t \text{ (s)} < 1$
Longueur de jambe Position du pied	Taille patient Flexion plantaire ou dorsale Rotation interne ou externe Hauteur	de 1,40 à 1,90 m
Réglages	Manuels	
Accès visuel direct		
Rigidité		
Encombrement	82*30*30 cm	
Réseau Electrique	De 100 à 240 Volts 50/60 Hz	
Dimensions	60*30*30 cm	
Poids	11,2 Kg	
Matériaux : Tubulures Coques	Acier chromé ou peint Plastique	

5. DESCRIPTION DES FONCTIONS DE L'ATTELLE DE GENOU

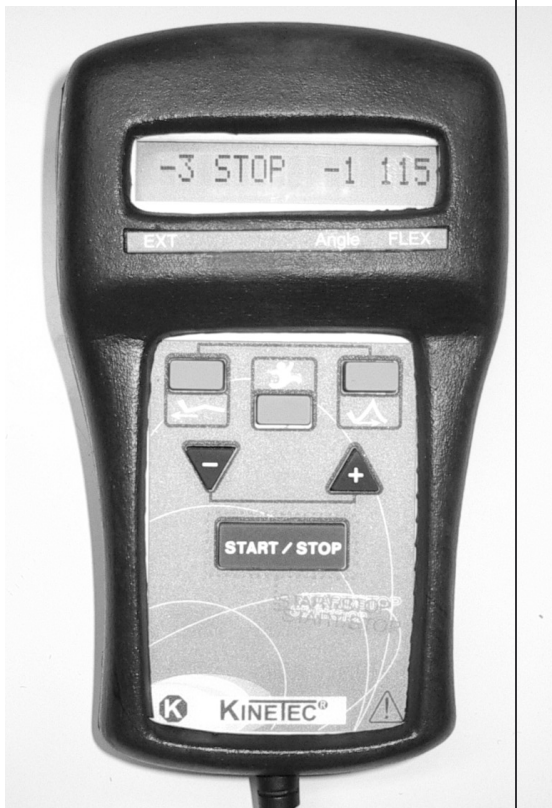
5.1 Schéma fonctionnel de l'attelle de genou :



5.2 Fonction F1 : « Gérer le fonctionnement de l'attelle »

Cette fonction est réalisée par 4 éléments de l'attelle :

le boîtier de commande :



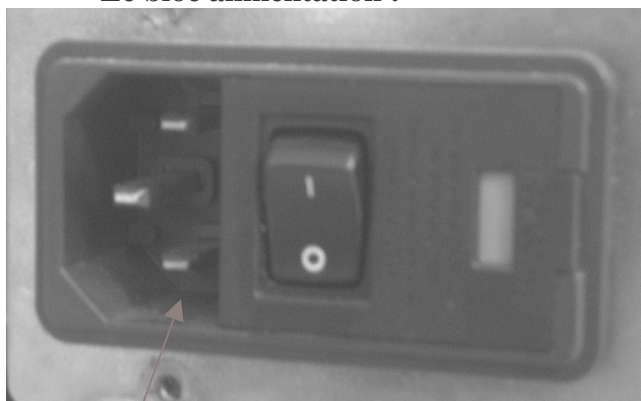
le capteur de l'angle du genou :



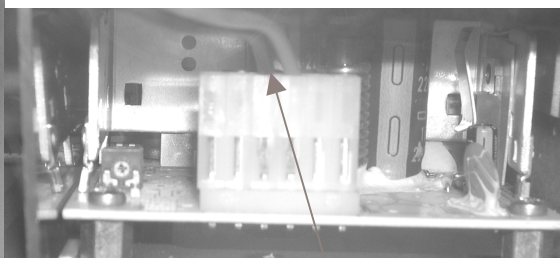
le moteur :



Le bloc alimentation :



Energie électrique



V_{BAT} : alimentation +12V

Entrées :

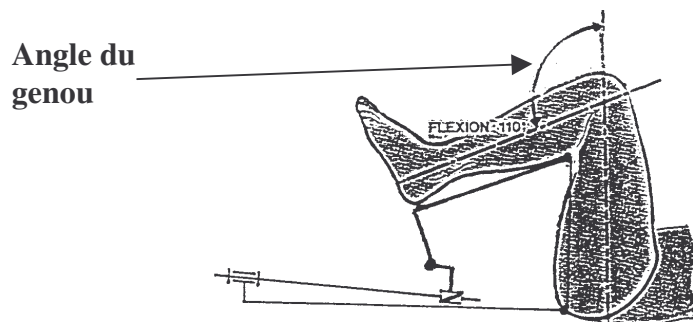
Energie électrique : tension en provenance du réseaux EDF. Différence de potentiel sinusoïdale alternative de valeur efficace 230V, et de fréquence 50Hz.

Marche/Arrêt : action du patient sur une touche du boîtier de commande afin d'arrêter le mouvement de l'attelle. Un second appui permet d'enclencher de nouveau le mouvement de l'attelle mais dans le sens opposé.

Réglages : action du personnel médical sur les touches du boîtier de commande afin de régler le fonctionnement de l'attelle en fonction du patient. Les différents réglages sont les suivants :

- réglage de la limite d'extension (-3° à 110°) précision du réglage de $\pm 1^{\circ}$,
- réglage de la limite de flexion (2° à 115°) précision du réglage de $\pm 1^{\circ}$,
- réglage de la vitesse du mouvement (1 à 5) ($50^{\circ}/\text{min}$ à $150^{\circ}/\text{min}$), précision du réglage de $25^{\circ}/\text{min}$.

Angle du genou : angle permettant de connaître l'état actuel du mouvement de l'attelle.



Sorties :

Rotation du moteur : sa vitesse dépend des réglages effectués par le personnel médical.

Visualisation : visualisation des différents réglages réalisés à l'aide d'un afficheur LCD. Cet afficheur affiche en permanence l'angle réalisé par le genou ainsi que les limites de flexion et d'extension. Lors des réglages des limites de flexion et d'extension cet afficheur affiche l'évolution des réglages.

Fonction de transfert :

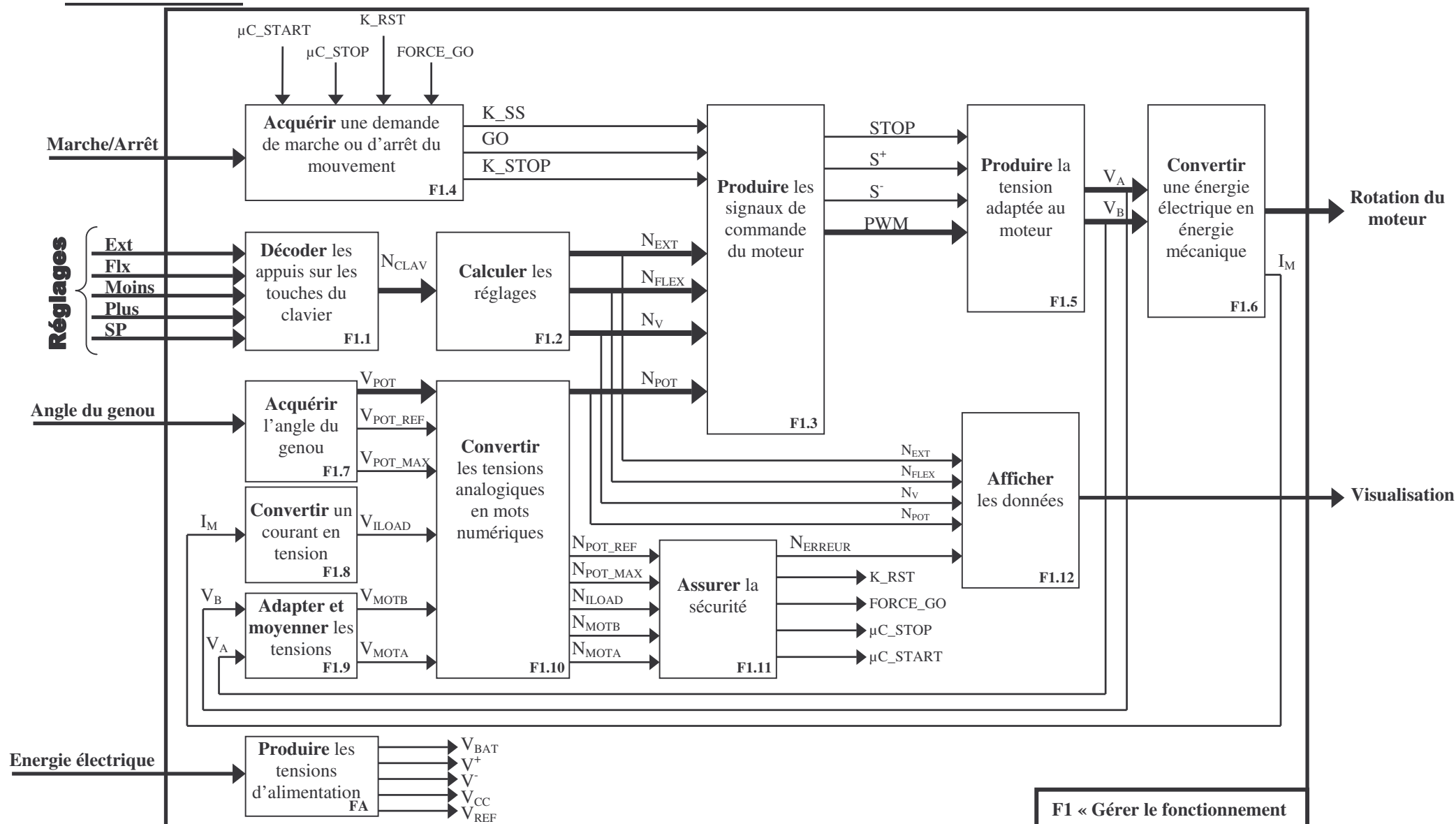
F1 « Gérer le fonctionnement de l'attelle » permet d'acquérir les réglages du personnel médical et de calculer en permanence l'angle courant du genou.

En fonction des réglages du personnel médical et de l'angle du genou, cette fonction permet d'actionner la rotation du moteur à vitesses différentes et dans les deux sens (flexion et extension).

Lorsque l'angle courant du genou arrive aux limites de flexion et d'extension, un arrêt de la rotation du moteur durant une seconde est produite. Puis la rotation du moteur change de sens.

A tout moment cette fonction permet d'arrêter le moteur à la demande du patient par un premier appui sur Marche/Arrêt, puis d'actionner la rotation du moteur dans le sens opposé par un deuxième appui sur Marche/Arrêt.

6. DESCRIPTION DES SOUS-FONCTIONS DE F1 « GÉRER LE FONCTIONNEMENT DE L'ATTELLE » :



6.1 Description de F1.1 : « Décoder les appuis sur les touches du clavier »**Entrées :**

Réglages : (Ext, Flx, Moins, Plus, SP) : actions du personnel médical sur les touches du boîtier de commande correspondantes :

-Ext : l'action sur cette touche permet de sélectionner le réglage de la limite de l'extension,

-Flx : l'action sur cette touche permet de sélectionner le réglage de la limite de flexion,

-Moins : l'action sur cette touche permet de décrémenter le réglage sélectionné,

-Plus : l'action sur cette touche permet d'incrémenter le réglage sélectionné,

-SP : l'action sur cette touche permet de sélectionner le réglage de la vitesse.

Sortie :

N_{CLAV} : variable logicielle sur 8 bits permettant de connaître la touche qui a été appuyée.

Fonction de transfert :

Les bits de la variable logicielle **N_{CLAV}** correspondent à une touche suivant les affectations suivantes :

N_{CLAV} :

	b7	b6	b5	b4	b3	b2	b1	b0
Touches correspondantes	X	X	X	SP	Plus	Moins	Flx	Ext

On mettra à un le bit correspondant si une touche est appuyée :

Touche appuyée	Aucune	Ext	Flx	Moins	Plus	SP
N_{CLAV}	\$00	\$01	\$02	\$04	\$08	\$10

De plus cette fonction bloque toutes les touches du clavier lorsque l'on appui simultanément sur les touches **Plus** et **Moins**. Lorsque l'on appui de nouveau simultanément sur les touches **Plus** et **Moins**, le clavier est débloqué.

6.2 Description de F1.2 : « Calculer les réglages »**Entrée :**

N_{CLAV} : variable logicielle sur 8 bits permettant de connaître la touche qui a été appuyée.

Sorties :

N_{EXT} : variable logicielle sur 8 bits correspondant à l'angle limite d'extension.

N_{FLEX} : variable logicielle sur 8 bits correspondant à l'angle limite de flexion.

N_V : variable logicielle sur 8 bits correspondant à la vitesse sélectionnée.

Fonction de transfert :

En fonction du code clavier **N_{CLAV}** cette fonction modifie les variables logicielles de sorties **N_{FLEX}**, **N_{EXT}** et **N_V**. Ensuite ces données sont sauvegardées en mémoire pour une utilisation ultérieure.

6.3 Description de F1.3 :« Produire les signaux de commande du moteur »

Entrées :

K_SS : différence de potentiel logique correspondant à l'appui sur la touche Start/Stop.

-**K_SS=0**, alors la touche Start/Stop n'est pas appuyée,

-**K_SS=1**, alors la touche Start/Stop est appuyée.

K_STOP : différence de potentiel logique indiquant si c'est le premier appui ou le second appui sur Start/Stop :

-au premier appui sur Start/Stop, **K_STOP** passe à 1.

-au second appui sur Start/Stop, **K_STOP** repasse à 0.

GO : différence de potentiel logique indiquant que le moteur doit être arrêter.

-**GO=0**, au premier appui sur Start/Stop (arrêt du moteur),

-**GO=1**, au second appui sur Start/Stop (le moteur peut de nouveau fonctionner).

N_POT : variable logicielle sur 8 bits correspondant à l'angle courant du genou

N_EXT : variable logicielle sur 8 bits correspondant à l'angle limite d'extension.

N_FLEX : variable logicielle sur 8 bits correspondant à l'angle limite de flexion.

N_V : variable logicielle sur 8 bits correspondant à la vitesse sélectionnée.

Sorties :

PWM : différence de potentiel de forme rectangulaire 0V-5V, de fréquence 31,25kHz et de rapport cyclique variable. Le rapport cyclique dépend de la vitesse sélectionnée.

S⁺ : différence de potentiel logique permettant de sélectionner le sens de rotation positif du moteur (sens de la flexion).

Cette différence de potentiel est active sur un niveau logique 1 (si **S⁺=1**, alors le moteur tourne dans le sens positif).

S⁻ : différence de potentiel logique permettant de sélectionner le sens de rotation négatif du moteur (sens de l'extension).

Cette différence de potentiel est active sur un niveau logique 1 (si **S⁻=1**, alors le moteur tourne dans le sens négatif).

STOP : différence de potentiel logique permettant de freiner le moteur.

Cette différence de potentiel est active sur un niveau logique 1 (si **STOP=1**, alors on réalise un freinage du moteur).

Attention : pour que ce freinage soit valide il faut que les différence de potentiel logiques **S⁺** et **S⁻** soient toutes les deux à « 0 ».

Fonction de transfert :

Cette fonction fait varier le rapport cyclique de la différence de potentiel **PWM** en fonction des variables **N_V** (correspondant à la vitesse) et **N_POT** correspondant à l'angle du genou courant. En effet même pour une vitesse sélectionnée le rapport cyclique varie en fonction de l'angle du genou (ce qui correspond aux difficultés de flexion et d'extension lors de la rééducation).

En comparant **N_POT** avec **N_EXT** et **N_FLEX** cette fonction fixe les différences de potentiel logique **S⁺** et **S⁻** à « 1 » ou à « 0 ».

Lorsque **N_POT** est égal à **N_FLEX** ou à **N_EXT** cette fonction fixe **S⁺** et **S⁻** à « 0 » puis passe **STOP** à 1 pour freiner le moteur. **STOP** reste à « 1 » pendant une seconde ensuite les différences de potentiel **S⁺** et **S⁻** sont fixées de manière à tourner dans l'autre sens.

A tout moment la passage à « 0 » de **GO** arrête le moteur, et fixe **S⁺** et **S⁻** à « 0 » et **STOP** à 1.

6.4 Description de F1.4:« Acquérir la demande de Marche/Arrêt du mouvement »

Entrées :

Marche/Arrêt : action du patient sur la touche du clavier Start/Stop :

- le premier appui, permet de demander un arrêt du mouvement l'attelle,
- un deuxième appui permet de remettre en mouvement l'attelle mais dans le sens opposé.

μC_STOP : différence de potentiel logique permettant de demander un arrêt de l'attelle lorsqu'une anomalie est détectée. Cette différence de potentiel est active sur un niveau logique « 1 ».

μC_START : différence de potentiel logique permettant de demander un remise en route de l'attelle lorsqu'il n'y a plus d'anomalie. Cette différence de potentiel est active sur un niveau logique « 1 ».

Sorties :

K_SS : différence de potentiel logique correspondant à l'appui sur la touche Start/Stop.

-**K_SS=0**, alors la touche Start/Stop n'est pas appuyée,

-**K_SS=1**, alors la touche Start/Stop est appuyée.

K_STOP : différence de potentiel logique indiquant si c'est le premier appui ou le second appui sur Start/Stop :

-au premier appui sur Start/Stop, **K_STOP** passe à 1.

-au second appui sur Start/Stop, **K_STOP** repasse à 0.

GO : différence de potentiel logique indiquant que le moteur doit être arrêter.

-**GO=0**, au premier appui sur Start/Stop ou μC_STOP passe à « 1 » (arrêt du moteur),

-**GO=1**, au second appui sur Start/Stop ou μC_START passe à « 1 » (le moteur peut de nouveau fonctionner).

6.5 Description de F1.5 : « Produire la tension adaptée au moteur »

Entrées :

PWM : différence de potentiel de forme rectangulaire 0V-5V, de fréquence 31,25kHz et de rapport cyclique variable. Le rapport cyclique dépend de la vitesse sélectionnée.

S⁺ : différence de potentiel logique permettant de sélectionner le sens de rotation positif du moteur (sens de la flexion).

Cette différence de potentiel est active sur un niveau logique 1 (si **S⁺=1**, alors le moteur tourne dans le sens positif).

S⁻ : différence de potentiel logique permettant de sélectionner le sens de rotation négatif du moteur (sens de l'extension).

Cette différence de potentiel est active sur un niveau logique 1 (si **S⁻=1**, alors le moteur tourne dans le sens négatif).

STOP : différence de potentiel logique permettant de freiner le moteur.

Cette différence de potentiel est active sur un niveau logique 1 (si **STOP=1**, alors on réalise un freinage du moteur).

Attention : pour que ce freinage soit valide il faut que les différence de potentiel logiques **S⁺** et **S⁻** soient toutes les deux à « 0 ».

Sorties :

V_A : différence de potentiel analogique qui dépend du sens de rotation que l'on souhaite commandé :

- arrêt : $V_A=0V$,
- sens positif (sens de la flexion) : $V_A=+12V$,
- sens négatif (sens de l'extension) :
 - sa forme est rectangulaire,
 - sa fréquence est fixe égale à 31.25kHz,
 - son rapport cyclique est variable selon le rapport cyclique de **PWM**,
 - son amplitude est (0V)-(+12V)

V_B : différence de potentiel analogique qui dépend du sens de rotation que l'on souhaite commandé :

- arrêt : $V_B=0V$,
- sens positif (sens de la flexion) :
 - sa forme est rectangulaire,
 - sa fréquence est fixe égale à 31.25kHz,
 - son rapport cyclique est variable selon le rapport cyclique de **PWM**,
 - son amplitude est (0V)-(+12V)
- sens négatif (sens d'extension) : $V_B=+12V$,

Commande du moteur=(V_A-V_B) : différence de potentiel permettant de commander le moteur.

Cette différence de potentiel possède les caractéristiques suivantes :

- sa forme est rectangulaire,
- sa fréquence est fixe égale à 31.25kHz,
- son rapport cyclique est variable selon la vitesse sélectionnée,
- sa polarité dépend du sens de commande du moteur :
 - dans le sens positif (sens de la flexion), c'est un signal rectangulaire d'amplitude (0V)-(+12V),
 - dans le sens négatif (sens de l'extension), c'est un signal rectangulaire d'amplitude (0V)-(-12V),
 - à l'arrêt, (V_A-V_B)=0V.

6.6 Description de F1.6 : « Convertir une énergie électrique en énergie mécanique »

Entrées :

V_A , V_B , **Commande du moteur** : voir description ci-dessus.

Sorties :

Rotation du moteur : sa vitesse dépend du rapport cyclique de la **commande du moteur**=(V_A-V_B).

I_M : courant circulant dans le moteur.

6.7 Description de F1.7 : « Acquérir l'angle du genou »

Entrée :

angle du genou : grandeur physique correspondant à l'angle du genou, cet angle peut varier de -3° à 115° .

Sorties :

V_{POT} : différence de potentiel analogique proportionnelle à l'angle du genou.

$$0,14V \leq V_{POT} \leq 1,78V$$

$V_{POT}=0,14V$ correspond à un angle de -3° .

$V_{POT}=1,78V$ correspond à un angle de 115° .

V_{POT_REF} : différence de potentiel analogique correspondant à l'alimentation du capteur d'angle et égale à **5V** lors d'un fonctionnement normal. Permet d'indiquer si le capteur est bien alimenté.

V_{POT_MAX} : différence de potentiel analogique fixe après réglage correspondant à la valeur maximale que le capteur d'angle puisse fournir. Permet d'indiquer qu'il n'y a pas de défauts sur le capteur d'angle. La plage de réglage est la suivante :

$$1,85V \leq V_{POT\_MAX} \leq 2,78V$$

6.8 Description de F1.8 : « Convertir un courant en tension »

Entrée :

I_M : courant circulant dans le moteur.

Sortie :

V_{ILOAD} : différence de potentiel analogique proportionnelle au courant I_M .

$$V_{ILOAD}=2,2 \times I_M.$$

6.9 Description de F1.9 : « Adapter et moyenner les tensions »

Entrées :

V_A : différence de potentiel analogique qui dépend du sens de rotation que l'on souhaite commandé :

-arrêt : $V_A=0V$,

-sens positif (sens de la flexion) : $V_A=+12V$,

-sens négatif (sens de l'extension) :

-sa forme est rectangulaire,

-sa fréquence est fixe égale à 31.25kHz,

-son rapport cyclique est variable selon le rapport cyclique de **PWM**,

-son amplitude est (0V)-(+12V)

V_B : différence de potentiel analogique qui dépend du sens de rotation que l'on souhaite commandé :

-arrêt : $V_B=0V$,

-sens positif (sens de la flexion) :

-sa forme est rectangulaire,

-sa fréquence est fixe égale à 31.25kHz,

-son rapport cyclique est variable selon le rapport cyclique de **PWM**,

-son amplitude est (0V)-(+12V)

-sens négatif (sens d'extension) : $V_B=+12V$,

Sorties :

V_{MOTA} : différence de potentiel analogique proportionnelle à $\langle V_A \rangle$. $V_{MOTA} = \frac{1}{3} \times \langle V_A \rangle$.

V_{MOTB} : différence de potentiel analogique proportionnelle à $\langle V_B \rangle$. $V_{MOTB} = \frac{1}{3} \times \langle V_B \rangle$.

Fonction de transfert :

Cette fonction permet d'adapter les différences de potentiel $V_{A\text{MAX}}=+12\text{V}$ et $V_{B\text{MAX}}=+12\text{V}$ aux entrées de F1.10 « Convertir des tensions analogiques en mots numériques ».

Elle permet également d'acquérir une image de la valeur moyenne de V_A et V_B .

Ceci permet de savoir si un problème apparaît sur la commande du moteur et sur le sens de rotation du moteur.

6.10 Description de F1.10 : « Convertir les tensions analogiques en mots numériques »

Entrées :

V_{MOTA} : différence de potentiel analogique proportionnelle à $\langle V_A \rangle$. $V_{\text{MOTA}} = \frac{1}{3} \times \langle V_A \rangle$.

V_{MOTB} : différence de potentiel analogique proportionnelle à $\langle V_B \rangle$. $V_{\text{MOTB}} = \frac{1}{3} \times \langle V_B \rangle$.

V_{ILOAD} : différence de potentiel analogique proportionnelle au courant I_M .
 $V_{\text{ILOAD}} = 2,2 \times I_M$.

V_{POT} : différence de potentiel analogique proportionnelle à l'angle du genou.

$$0,14\text{V} \leq V_{\text{POT}} \leq 1,78\text{V}$$

$V_{\text{POT}} = 0,14\text{V}$ correspond à un angle de -3° .

$V_{\text{POT}} = 1,78\text{V}$ correspond à un angle de 115° .

$V_{\text{POT\_REF}}$: différence de potentiel analogique correspondant à l'alimentation du capteur d'angle et égale à 5V lors d'un fonctionnement normal. Permet d'indiquer si le capteur est bien alimenté.

$V_{\text{POT\_MAX}}$: différence de potentiel analogique fixe après réglage correspondant à la valeur maximale que le capteur d'angle puisse fournir. Permet d'indiquer qu'il n'y a pas de défauts sur le capteur d'angle. La plage de réglage est la suivante :

$$1,85\text{V} \leq V_{\text{POT\_MAX}} \leq 2,78\text{V}$$

Sorties :

N_{POT} : variable logicielle sur 8 bits correspondant à l'angle courant du genou.

$N_{\text{POT\_REF}}$: variable logicielle sur 8 bits correspondant à l'alimentation du capteur d'angle.

$N_{\text{POT\_MAX}}$: variable logicielle sur 8 bits correspondant à la valeur maximale que le capteur d'angle puisse fournir.

N_{ILOAD} : variable logicielle sur 8 bits correspondant au courant circulant dans le moteur.

N_{MOTA} : variable logicielle sur 8 bits correspondant à la commande d'un mouvement de flexion.

N_{MOTB} : variable logicielle sur 8 bits correspondant à la commande d'un mouvement d'extension.

6.11 Description de F1.11 : « Gérer la sécurité »

Entrées :

N_{ILOAD} : variable logicielle sur 8 bits correspondant au courant circulant dans le moteur.

N_{MOTA} : variable logicielle sur 8 bits correspondant à la commande d'un mouvement de flexion.

N_{MOTB} : variable logicielle sur 8 bits correspondant à la commande d'un mouvement d'extension.

N_{POT_REF} : variable logicielle sur 8 bits correspondant à l'alimentation du capteur d'angle.

N_{POT_MAX} : variable logicielle sur 8 bits correspondant à la valeur maximale que le capteur d'angle puisse fournir.

Sorties :

N_{ERREUR} : variable logicielle sur 8 bits correspondant à l'erreur détectée.

μC_STOP : différence de potentiel logique permettant de demander un arrêt de l'attelle lorsqu'une anomalie est détectée. Cette différence de potentiel est active sur un niveau logique « 1 ».

μC_START : différence de potentiel logique permettant de demander un remise en route de l'attelle lorsqu'il n'y a plus d'anomalie. Cette différence de potentiel est active sur un niveau logique « 1 ».

Fonction de transfert :

Les mots numériques **N_{POT_MAX}** et **N_{POT_REF}** permettent de **détecter** s'il y a un problème sur l'acquisition de l'**angle du genou**.

Le mot numérique **N_{ILOAD}** permet de **détecter** un courant trop important circulant dans le moteur. Si le courant dans le moteur est supérieur à **1,2A** alors on doit arrêter le moteur pendant 1s et **enclencher** la rotation du moteur dans l'autre sens.

Les mots numériques **N_{MOTA}** et **N_{MOTB}** permettent de **détecter** un problème sur la commande du moteur.

6.12 Description de F1.12 : « Afficher les données »

Entrées :

N_{POT} : variable logicielle sur 8 bits correspondant à l'angle courant du genou.

N_{EXT} : variable logicielle sur 8 bits correspondant à l'angle limite d'extension.

N_{FLEX} : variable logicielle sur 8 bits correspondant à l'angle limite de flexion.

N_V : variable logicielle sur 8 bits correspondant à la vitesse sélectionnée.

N_{ERREUR} : variable logicielle sur 8 bits correspondant à l'erreur détectée.

Sortie :

Visualisation : données visualisées grâce à un afficheur LCD.

Cet afficheur affiche en permanence l'angle courant du genou, l'angle limite de flexion et l'angle limite d'extension.

Lors d'une sélection d'un réglage de l'angle limite d'extension ou d'extension, l'angle en question clignote.

Lors d'une sélection d'un réglage de la vitesse l'afficheur affiche la vitesse.

Lors d'une erreur détectée (en fonction de la variable logicielle **N_{ERREUR}**), l'afficheur affiche l'erreur détectée :

- « SERVICE D1 » : anomalie sur la fonction mesurage de l'angle,
- « SERVICE D2 » : anomalie dans le pilotage du moteur et/ou de l'attelle,
- « SERVICE D3 » : anomalie sur le sens de rotation du moteur.

6.13 Description de FA : « Produire les tensions d'alimentation »

Entrée :

Energie électrique : tension en provenance du réseaux EDF. Différence de potentiel sinusoïdale alternative de valeur efficace 230V, et de fréquence 50Hz.

Sorties :

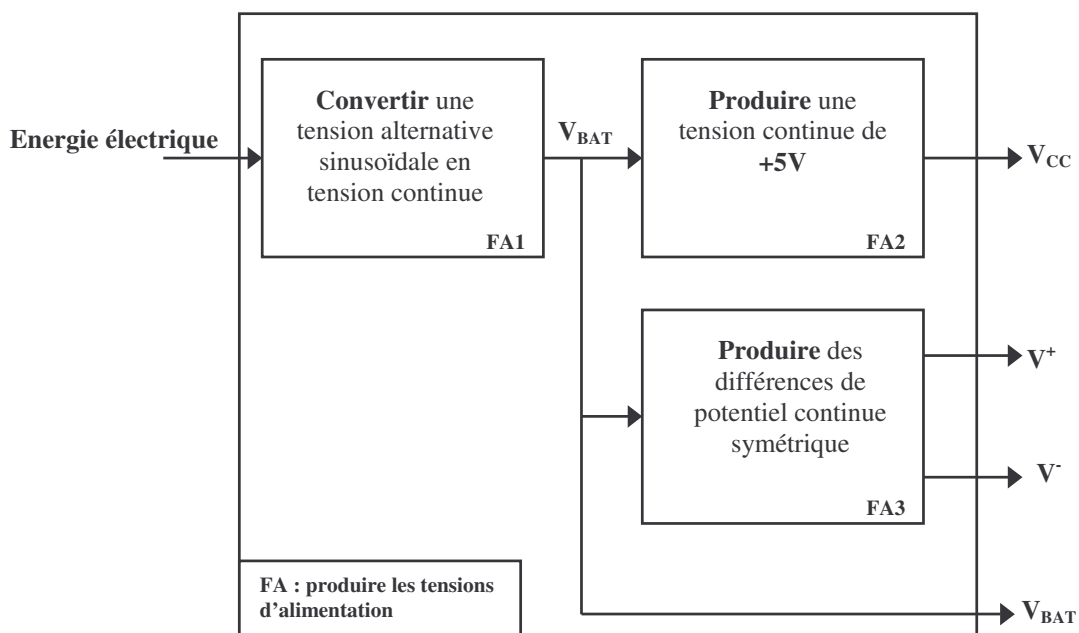
V_{BAT} : différence de potentiel analogique continue de **+12V**.

V^+ : différence de potentiel analogique continue de **+5V**.

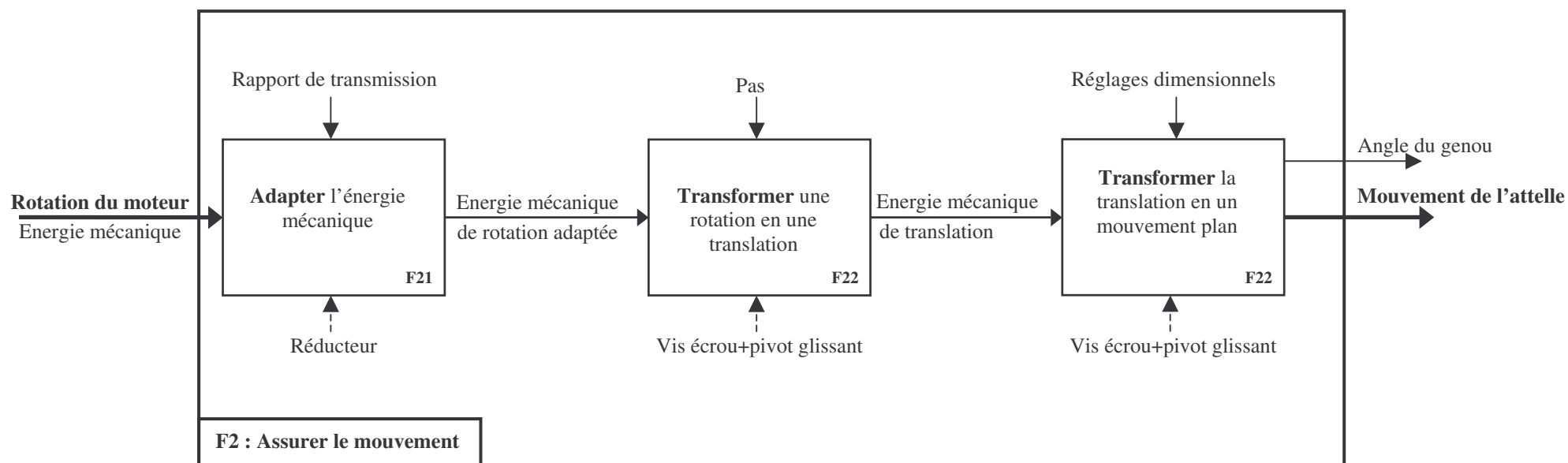
V^- : différence de potentiel analogique continue de **-5V**.

V_{CC} : différence de potentiel analogique continue de **+5V**

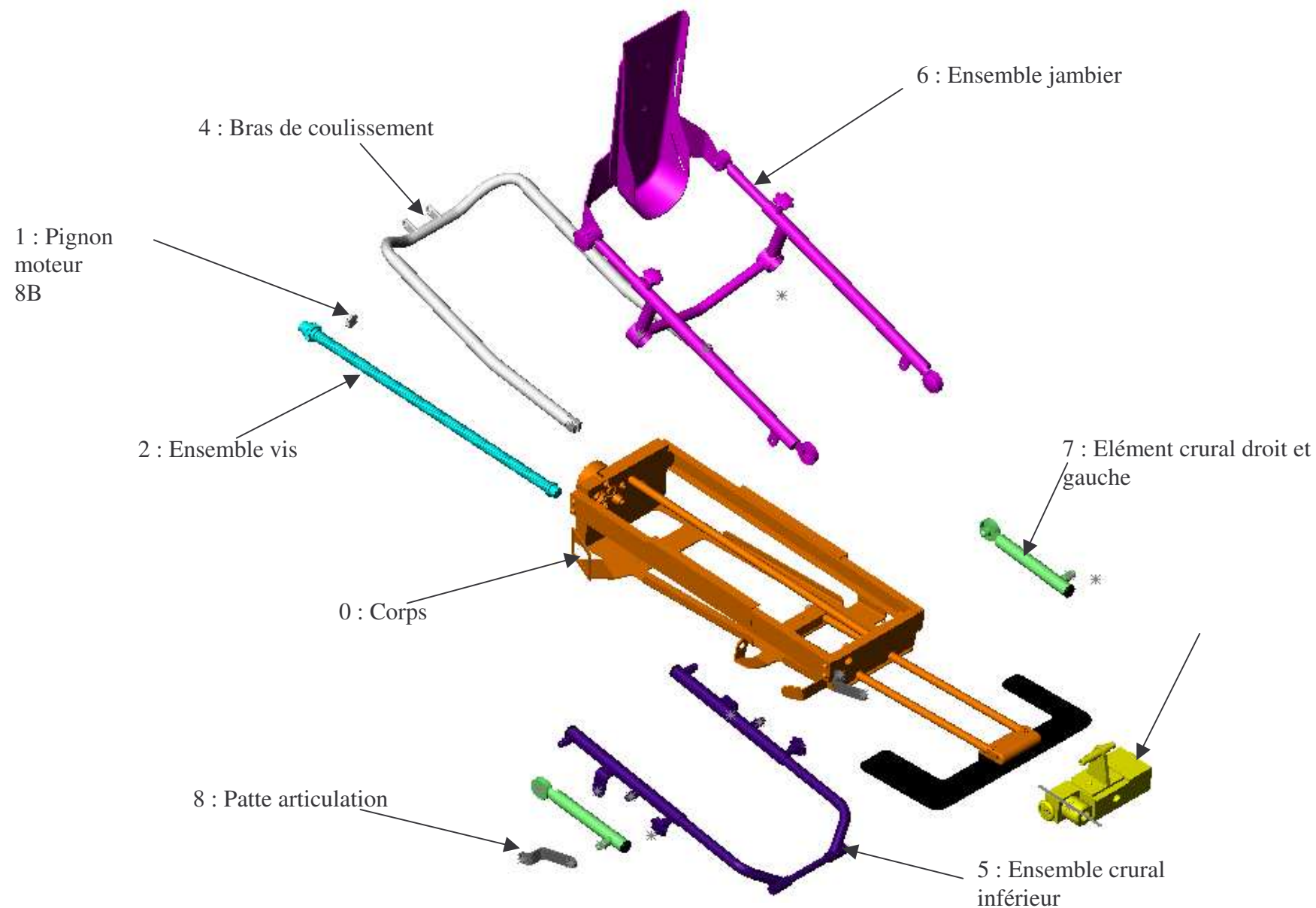
Afin de mieux comprendre comment sont produites ces différences de potentiel, voici la décomposition fonctionnelle de FA « **Afficher les données** » :

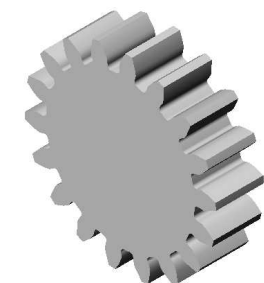
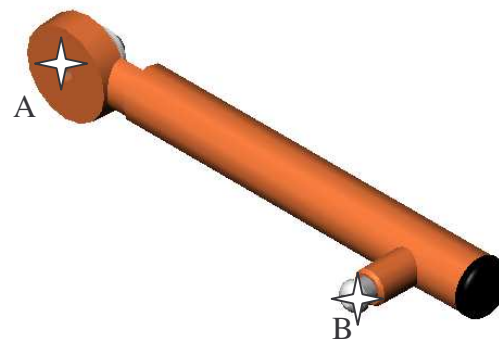


7. DESCRIPTION DES SOUS-FONCTIONS DE F2 « ASSURER LE MOUVEMENT » :

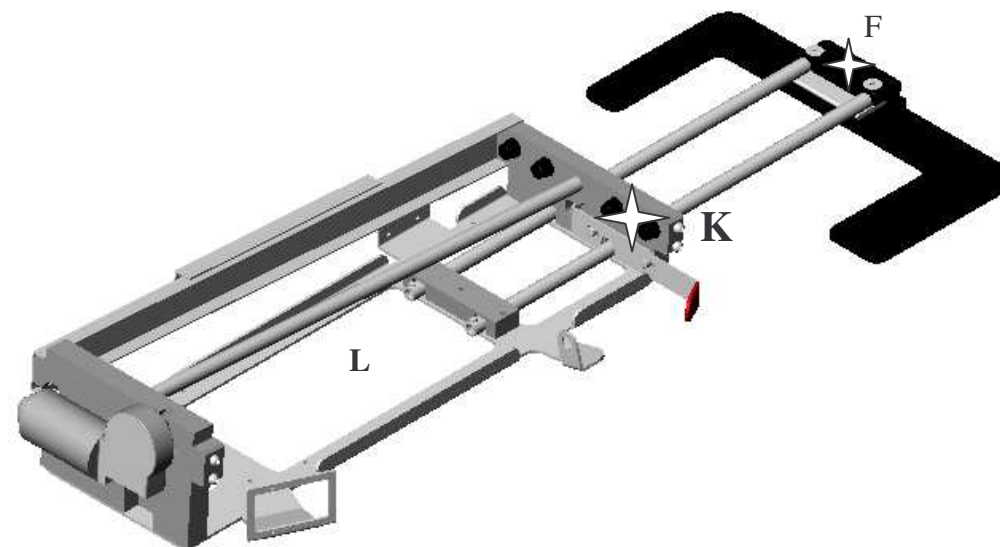
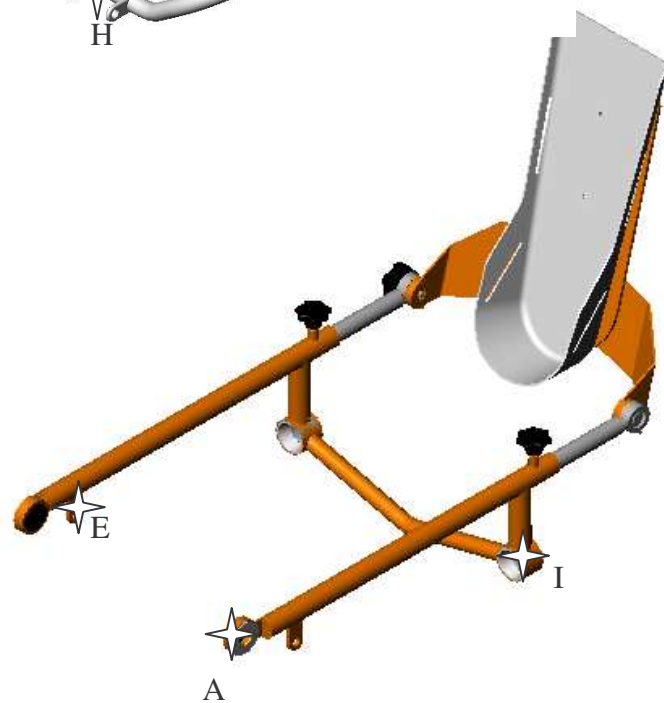


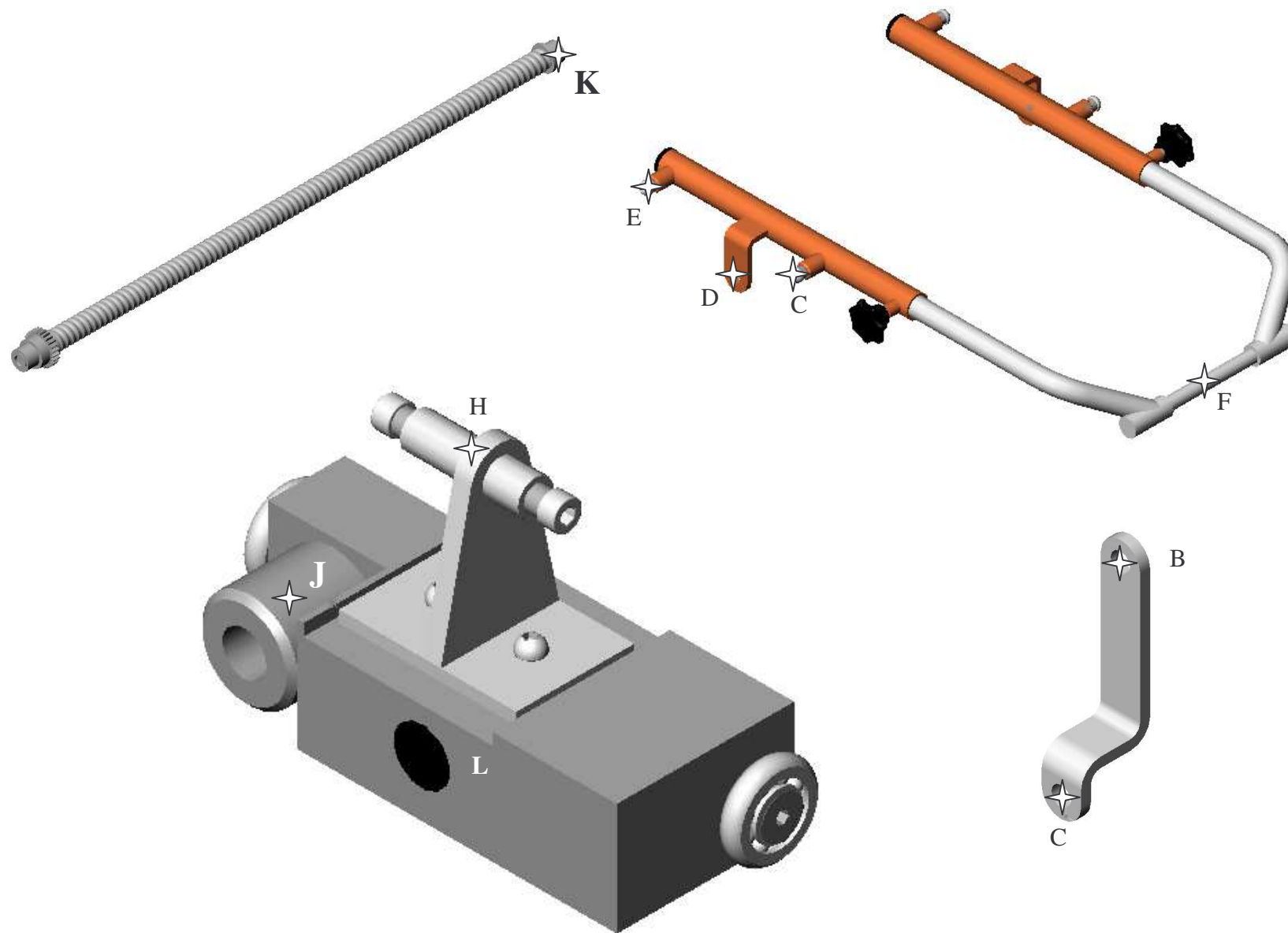
8. ECLATE DE L'ATTELLE DE GENOU AVEC LES GROUPES CINEMATiques :





Pignon moteur 8B





9. DIDACTISATION :

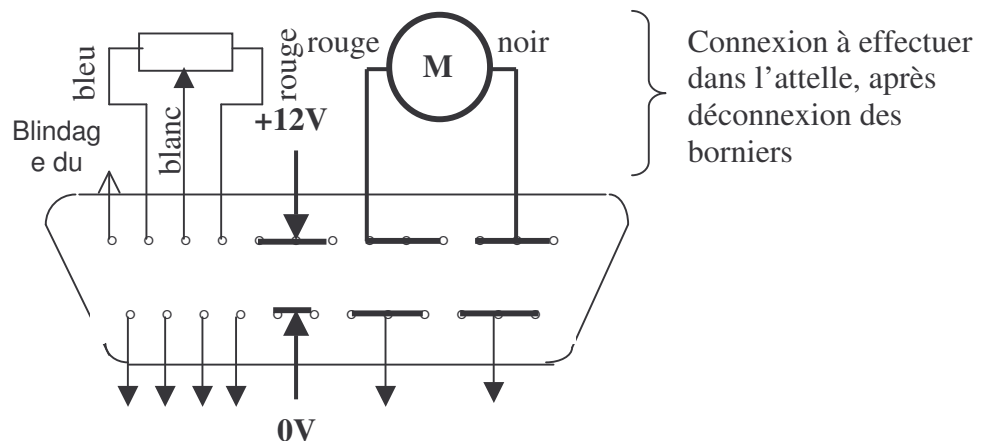
On a la possibilité d'utiliser l'attelle de deux manières différentes :

- fonctionnement avec le boîtier de commande,
- fonctionnement avec la carte didactisée.

9.1 Modification à apporter à l'attelle

Plan de connexion de la prise SUB 25 points (femelle) fixée sur l'attelle :

Vue de l'extérieur de l'attelle :

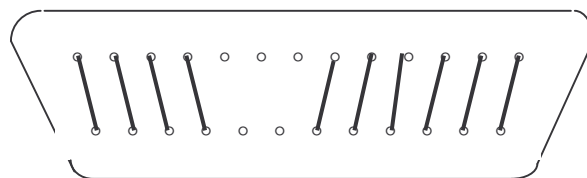


Vers les borniers (à l'intérieur de l'attelle vers le boîtier de commande) d'où ont été enlevés le potentiomètre de recopie et le moteur en respectant les branchements initiaux.

Tous ces câblages seront internes

Les alimentations (0V-12V) seront prises directement sur le bornier afin d'utiliser l'alimentation de l'attelle pour la carte didactique.

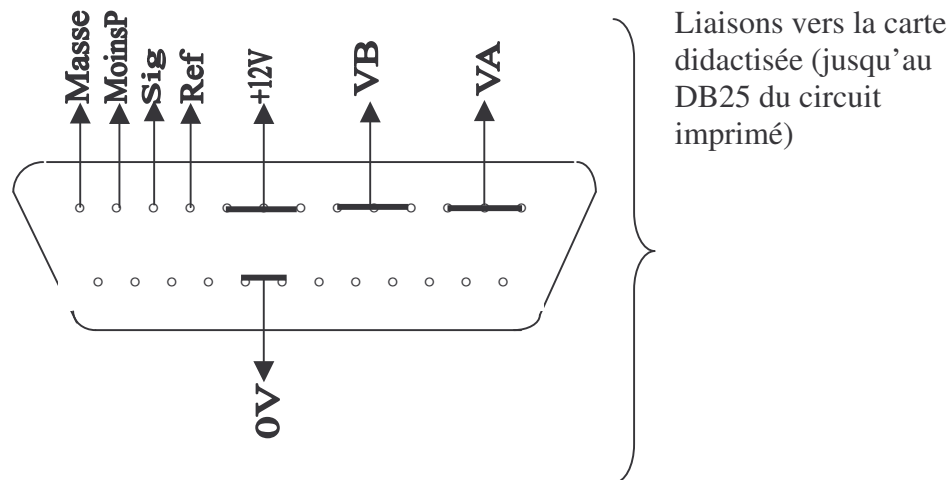
Plan de connexion de la prise SUB 25 points (mâle) servant à rétablir les connexions d'origine de l'attelle : (utile pour utiliser la commande d'origine)



Les connexions d'origine sont ainsi rétablies par cette prise (qui ne contient que les connexions représentées ci-dessus).

C'est le boîtier de commande qui gère le fonctionnement de l'attelle.

Plan de connexion de la prise SUB 25 points (mâle) servant à relier la carte didactisée sur l'attelle



9.2 Fonctionnement avec le boîtier de commande

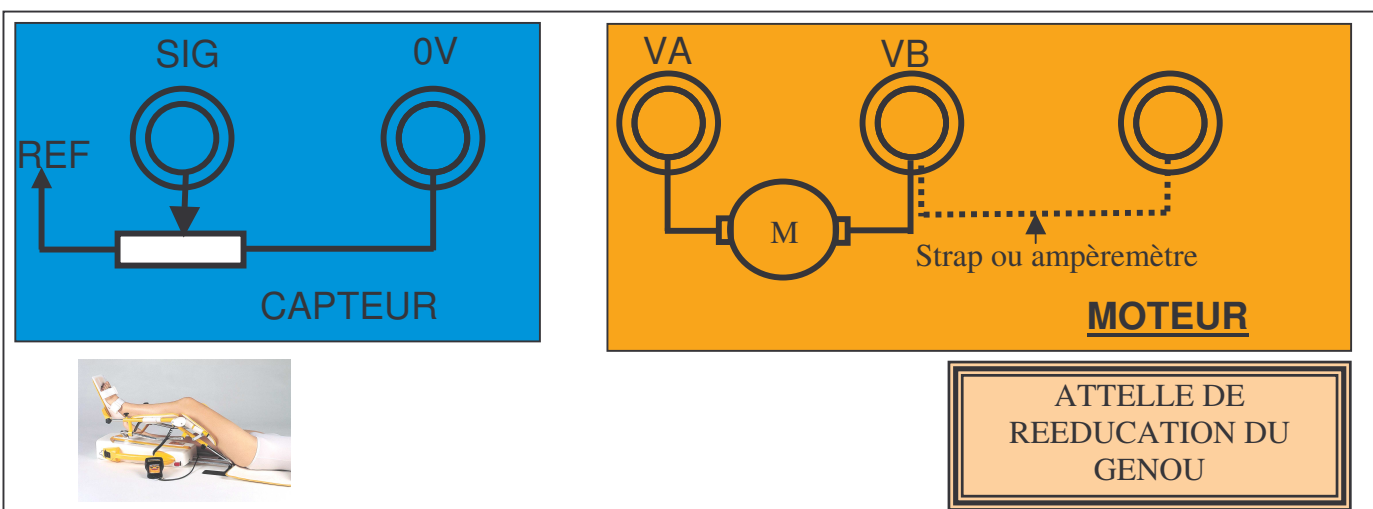
Pour que le boîtier de commande puisse fonctionner il faut connecter sur le connecteur DB25 de l'attelle, le DB25 réalisant les connexions avec le boîtier de commande

Sur la face avant de l'attelle sont présents différents points de mesure :

- tension moteur,
- courant moteur
- tension issue du capteur de l'angle du genou.

Attention : pour que l'attelle fonctionne, il faut que le strap de la mesure du courant soit présent.

Face avant de l'attelle représentant les points de mesures :



9.3 Fonctionnement avec la carte didactisée

La carte didactisée reprend la même structure que la carte industrielle, à la différence près que le microcontrôleur utilisé est un PIC16F877.

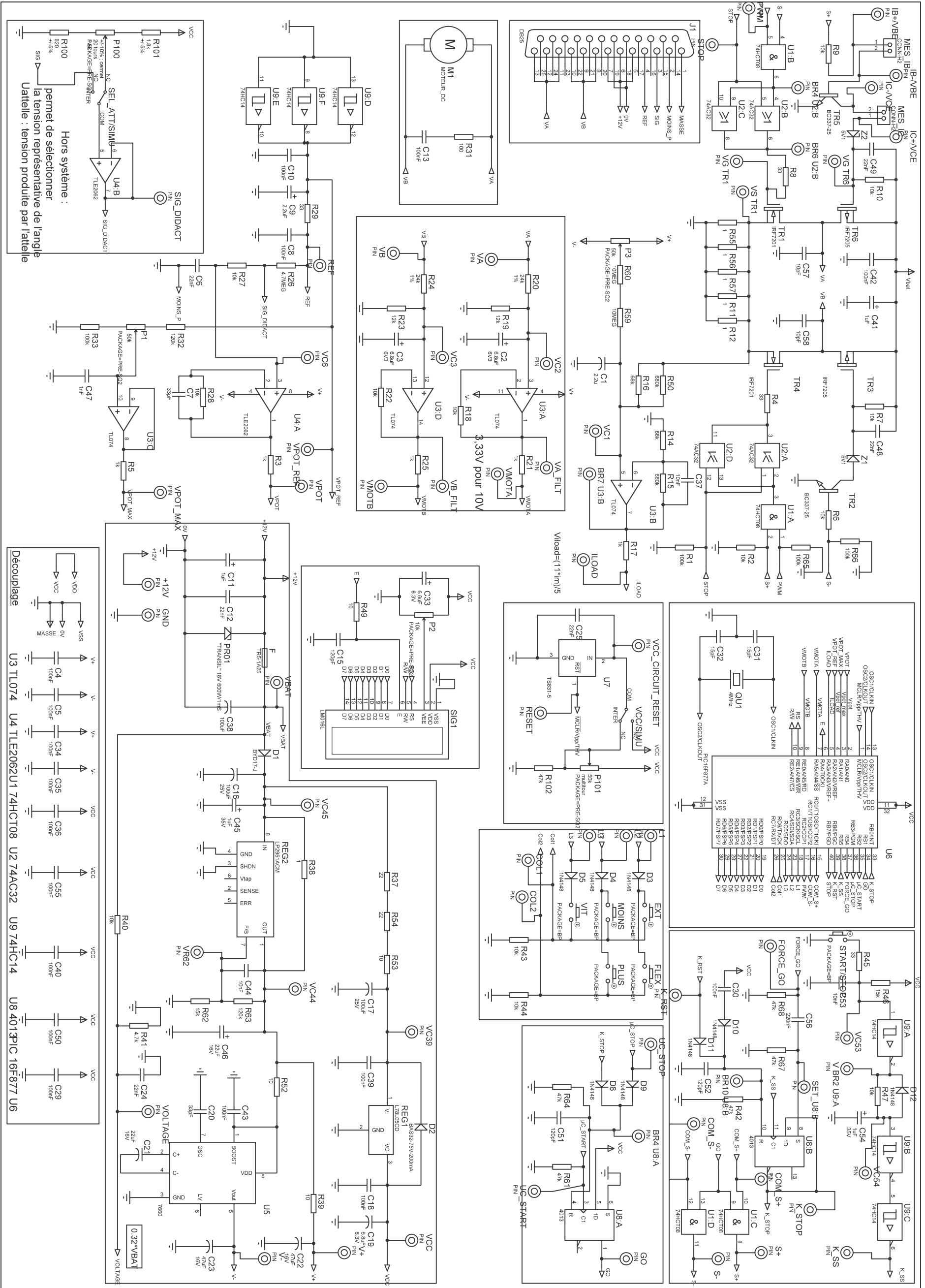
On a la possibilité de simuler une modification de l'angle du genou grâce à un potentiomètre (**P100**).

On a la possibilité de simuler une chute de l'alimentation en basculant l'interrupteur (**Vcc/Simu**) et en modifiant la valeur de Vcc grâce au potentiomètre (**P101**).

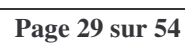
Des mesures des courants I_C et I_B sont réalisables sur le transistor bipolaire BC337-25 (**TR5**), en enlevant les cavaliers (**MES_IB** et **MES_IC**) et en y plaçant un ampèremètre.

Des points de mesures caractéristiques sont aussi présents sur cette carte.

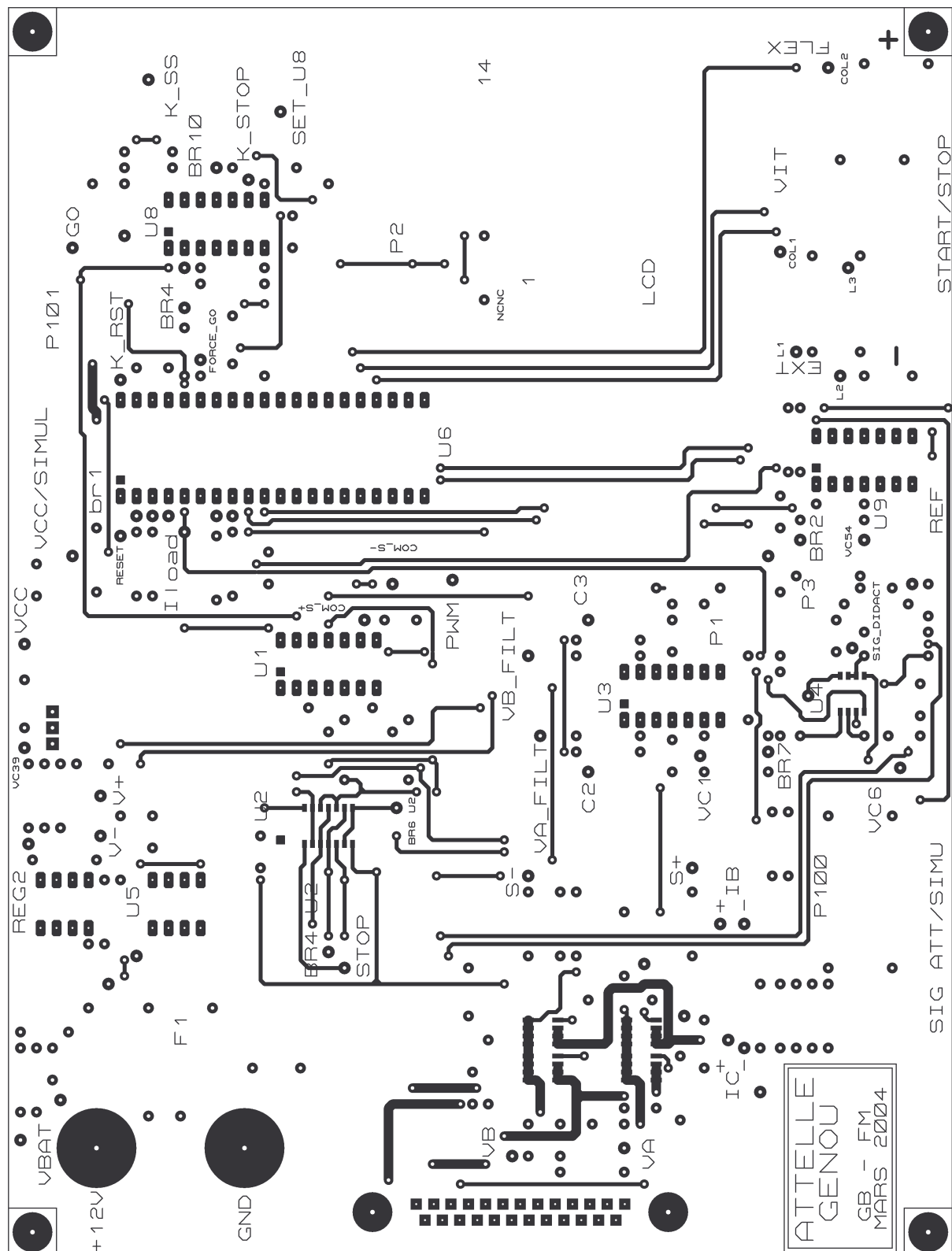
9.4.1 Schéma structurel de la carte didactisée



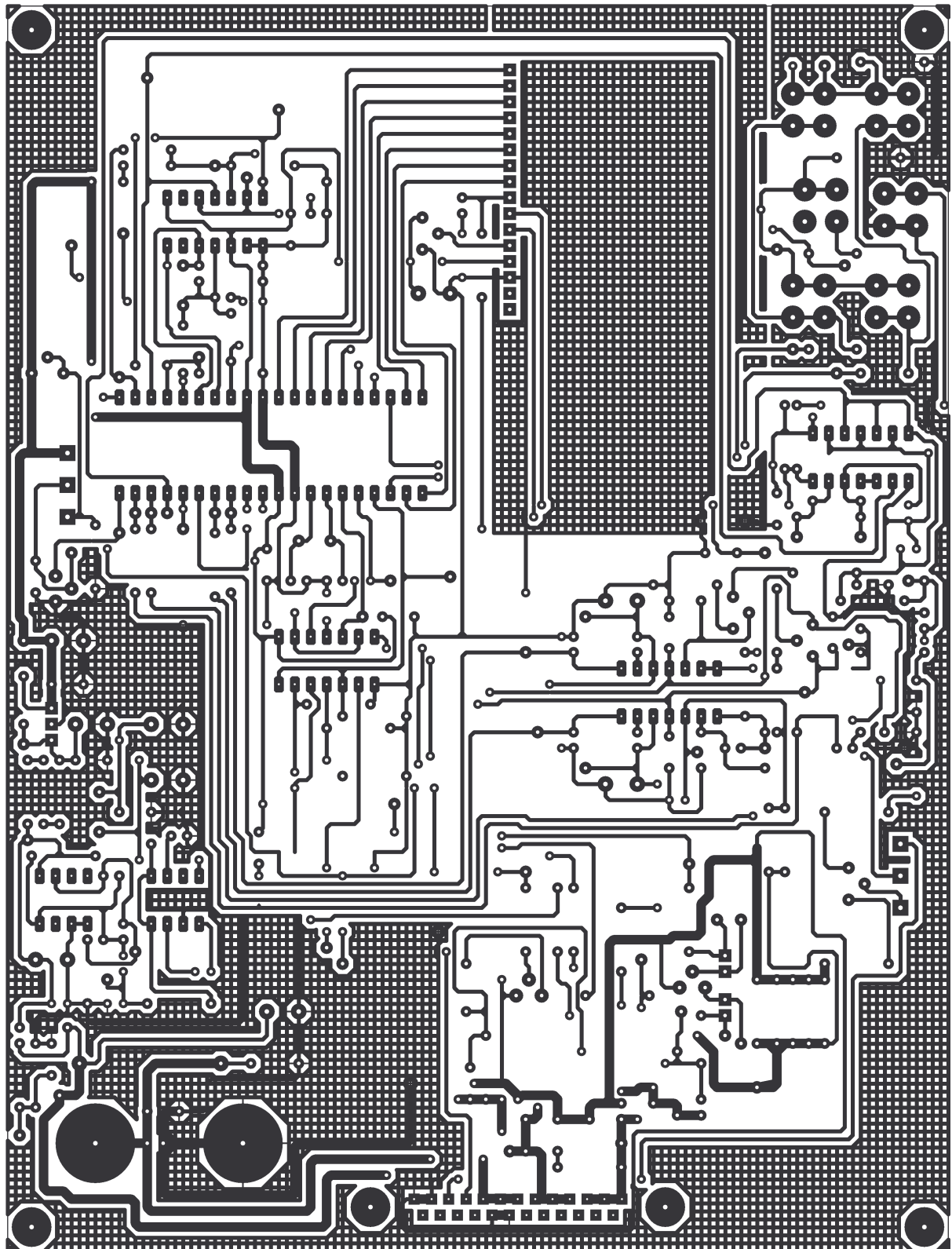
9.4.2 Implantation des composants



9.4.3 Côté composants



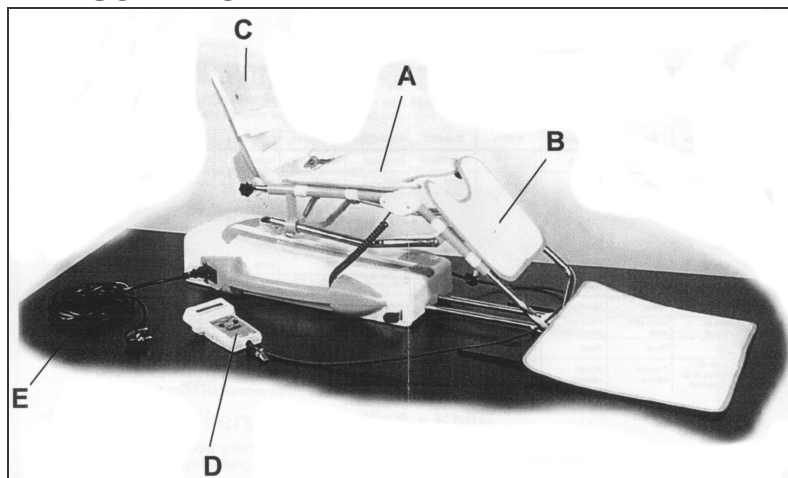
9.4.4 Côté cuivre



10. EXTRAIT DES DOCUMENTS TECHNIQUES DE KINETEC :

10.1 Extrait du manuel d'utilisation

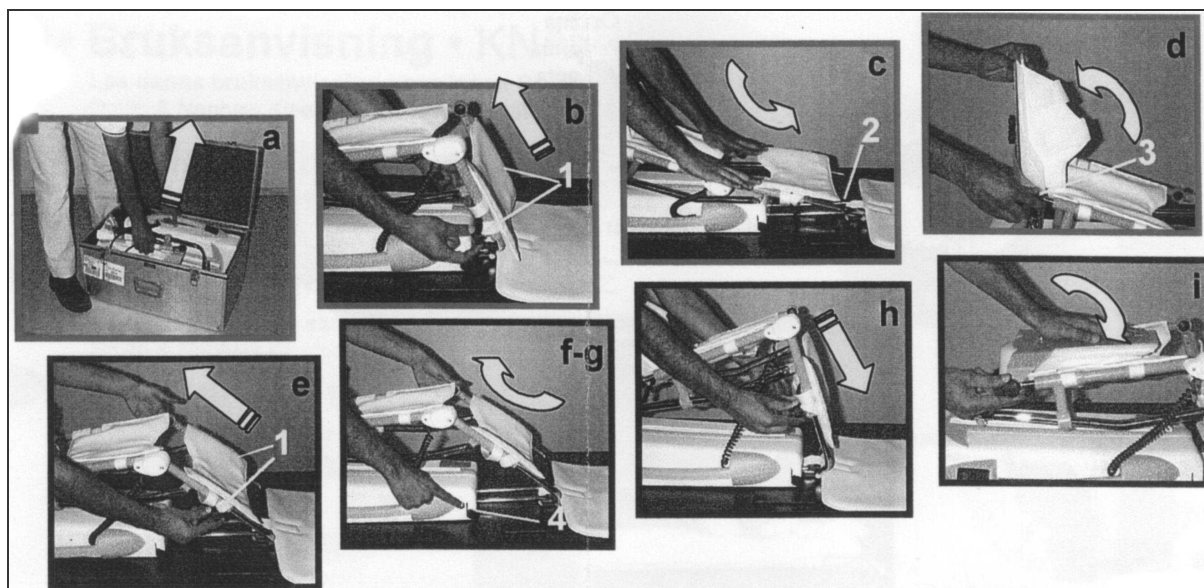
1- DESCRIPTION :



Le KINETEC Adventa est un appareil de mobilisation passive du genou et de la hanche en flexion-extension.

A - Berceau jambier • B - Berceau crural • C - Semelle articulée • D - Télécommande • E - Cordon secteur

2- DEBALLAGE - EMBALLAGE :



Déballage :

a – Sortir le KINETEC Adventa de son emballage.

b – Desserrer les 2 boutons noirs (1) et ajuster en position maximum le berceau crural, resserrer les 2 boutons.

c – Coulisser les rallonges d'attelle (2) jusqu'au blocage automatique (position verrouillée).

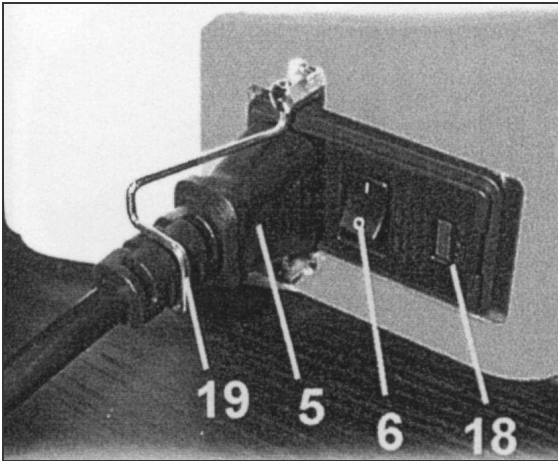
d – Desserrer le bouton noir (3) et redresser la planchette.

Le KINETEC Adventa est prêt à fonctionner.

Emballage :

- e- Desserrer les 2 boutons noirs (1) et ajuster en position maximum le berceau crural, resserrer les 2 boutons.
 - f- Stopper l'attelle à 0° (flèche sur l'étiquette de transport).
 - g- Tirer sur le bouton (4) et rentrer les rallonges d'attelle en soulevant par l'articulation du genou.
 - h-i- Régler la longueur crurale au minimum et pivoter la planchette.
 - j - Mettre le KINETEC *Adventa* dans son emballage.
- Le KINETEC *Adventa* est prêt à être expédié.**

3- BRANCHEMENT ELECTRIQUE : SECURITE D'ABORD :



Le KINETEC *Adventa* + est un appareil de type B, classe I.

Brancher le cordon secteur (5) au KINETEC *Adventa* + et à une prise secteur, bloquer le cordon à l'aide de l'anneau (19) (fonctionnement de 100 à 240 Vac 50/60Hz).

IMPORTANT

Vérifier que la prise de courant soit en bon état et apte à recevoir la fiche du cordon d'alimentation de l'attelle. Cette dernière est conforme aux normes en vigueur et comporte un logement pour mise à la terre. Cette fiche peut être branchée sur n'importe quelle prise de courant standard, qui toutefois, doit être munie d'une broche raccordée à la terre. Utiliser à cette fin, seulement le cordon d'origine livré avec le KINETEC.

Veillez à ce que les cordons restent toujours libres autour de l'appareil pour éviter de les endommager.

Changement des fusibles

Attention, remplacer les fusibles par le même type et le même calibre.

- entrée secteur T 500 mA 250V (6.3x32).
- télécommande T 1.25 A (TR5).

4- SECURITE :

Le praticien détermine le protocole et s'assure de sa bonne exécution (réglages, temps de séance et fréquence d'utilisation).

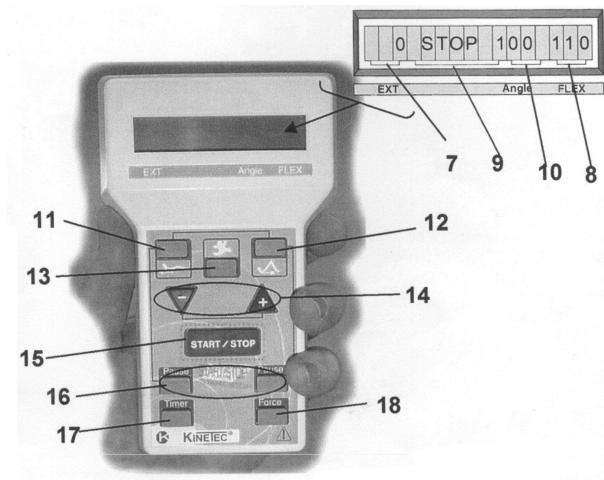
Le patient a assimilé la fonction marche/arrêt/inversion de la télécommande, voir paragraphe 5.

Le KINETEC *Adventa* + est conforme à la directive 89/336/CEE et à la norme IEC 601.1. il est marqué CE.

Le KINETEC *Adventa* + ne présente pas d'interférences magnétiques, électriques au autre types par rapport à d'autres appareils.

DANGER RISQUE D'EXPLOSIONS : le KINETEC *Adventa* + n'est pas prévu pour être utilisé avec du gaz anesthésique.

5- MISE EN ROUTE :



Actionner l'interrupteur (6).

L'afficheur indique

KINETEC

Blocage de la télécommande

Pour verrouiller la télécommande, appuyer simultanément sur les touches « + » et « - » et l'afficheur indique « LOCK », seule la lecture des valeurs d'utilisation reste possible et la fonction START/STOP.

Pour déverrouiller la télécommande appuyer simultanément sur les touches « + » et « - » et l'afficheur indique « UNLOCK ».

Nous vous conseillons de verrouiller la télécommande lors de la séance.

Afficheur

- 7- 3 caractères indiquent la limite d'EXTENSION.
- 8- 3 caractères indiquent la limite de FLEXION.
- 9- 8 caractères indiquent des messages (RUN, STOP, EXT, FLEX, SPEED, ETC..).
- 10- 3 caractères indiquent l'angle réel du KINETEC *Adventa* +.

Fonction des touches

- 11- Lecture ou sélection de la limite en EXTENSION de -5° à 115° .
- 12- Lecture ou sélection de la limite en FLEXION de 120° à 0° .
- 13- Lecture ou sélection de la vitesse de 5 à 1.
- 14- Ces touches permettent la diminution ou l'augmentation des valeurs de fonctionnement.
- 15- cette touche permet le départ, l'arrêt ou l'inversion du mouvement.

IMPORTANT : pour un maximum de sécurité, la télécommande doit toujours être confiée au patient.

6- CARACTERISTIQUES TECHNIQUES :

Produit :

Poids : 11.2 kg
Dimensions de l'attelle : 60cm x 30cm x 30cm.
Limites angulaires : de -5° à 120° .
Vitesses : de 50 à 150°/mn en fémur maxi.
Taille des patients : de 1,40m à 1,90m.

Electricité :

Tension d'alimentation : de 100 à 240V□.
Fréquence : 50/60Hz.
Puissance absorbée : 50VA.
Appareil de type B classe I.

Environnement :

Conditions de stockage / transport :

Température ambiante : -40°C à $+70^{\circ}\text{C}$.

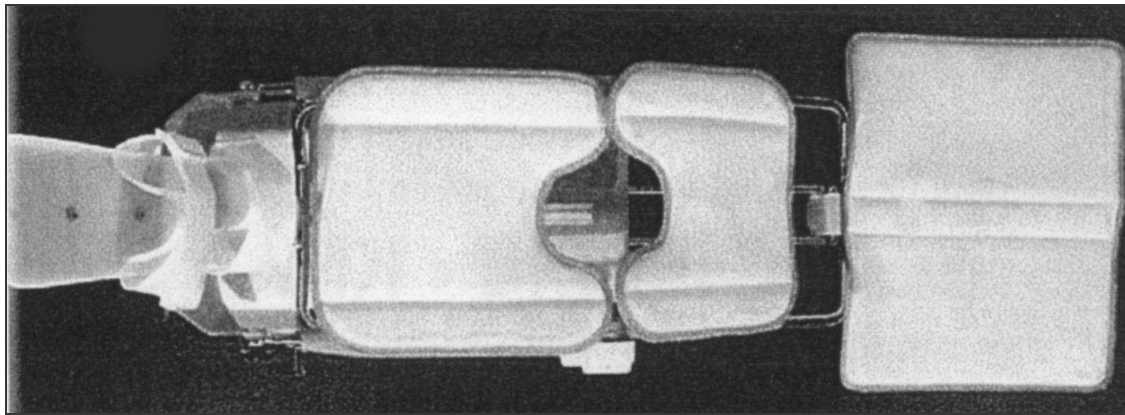
Humidité relative : jusqu'à 90%

Conditions d'utilisations :

Température ambiante : $+10^{\circ}\text{C}$ à $+40^{\circ}\text{C}$.

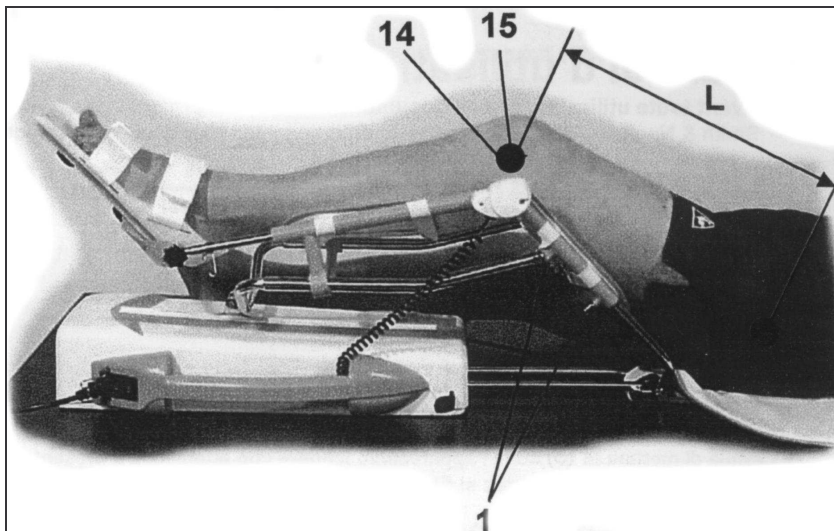
Humidité relative : jusqu'à 80%.

7- UTILISATION DE L'HABILLAGE HYGIENIQUE KINETEC



L'habillage hygiénique KINETEC a été spécialement conçu pour une mise en place rapide, une hygiène totale et un confort maximum du patient.
Positionner l'habillage comme indiqué sur le schéma ci-dessus.
ATTENTION : le manchon doit être orienté coté échancré vers l'articulation.

8- INSTALLATION DU PATIENT :

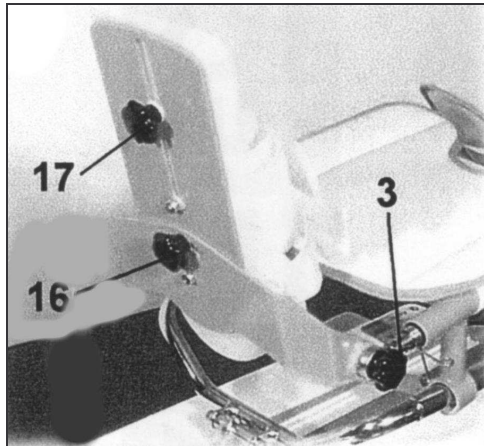


- Positionner le KINETEC *Adventa +*, dans une position antalgique pour le patient.
- Mesurer la longueur crurale (L) du patient et ajuster le berceau crural à cette mesure à l'aide des boutons (1).
- Installer le patient sur le KINETEC *Adventa +*, la longueur jambière se règle automatiquement.
- Sangler le pied

IMPORTANT

Régler le plus précisément possible l'axe d'articulation (14) du genou avec l'axe d'articulation (15) du KINETEC *Adventa +*.

9- REGLAGE DE LA SEMELLE ARTICULEE:



La semelle articulée permet le positionnement du pied en flexion plantaire ou dorsale et en rotation interne ou externe.

-Le bouton (3) permet le positionnement du pied en flexion plantaire ou dorsale.

-Le bouton (16) permet le positionnement du pied en rotation interne ou externe

-Le bouton (17) permet le réglage en hauteur du pied.

10-MAINTENANCE :

Après 2 000 heures de fonctionnement, le **KINETEC Adventa +** nécessite quelques opérations de graissage et d'entretien (graissage des articulations, de la butée à aiguille, et de la vis à bille si nécessaire). Cette opération d'entretien est signalée par la diode rouge (12) qui clignote à la mise sous tension.

Malgré cet avertissement, vous pouvez continuer à utiliser votre KINETEC en appuyant sur la touche START/STOP mais vous devez contacter votre spécialiste KINETEC le plus proche pour réaliser cette opération d'entretien.

Lorsque l'appareil n'est plus en état de fonctionner, veuillez nous le retourner ainsi que les accessoires pour destruction.

11- DEPANNAGE :

Une notice de pièces de rechange et/ou un catalogue technique sont à votre disposition sur simple demande auprès de votre distributeur KINETEC.

Après le branchement du cordon secteur sur une prise de courant et après la mise sous tension du KINETEC Adventa + au moyen de l'interrupteur (6) qui doit être sur la position I :

L'afficheur n'indique aucune information :

-Vérifier la présence de tension sur la prise secteur au moyen d'un autre appareil.

-Remplacer le ou les fusibles du connecteur (23) par le même type et calibre : 2 fusibles T 500 mA 250V (6,3X32).

Si l'afficheur n'indique toujours pas d'information, contacter votre spécialiste KINETEC le plus proche.

Après la mise sous tension de votre KINETEC au moyen de l'interrupteur (6) :

Votre KINETEC ne fonctionne pas et l'afficheur indique « 15 STOP 25 110 », appuyer à nouveau sur la touche « START/STOP ».

Votre KINETEC ne fonctionne toujours pas : contacter votre spécialiste KINETEC le plus proche.

Votre KINETEC ne fonctionne pas et l'afficheur indique :

- « SERVICE D1 » : anomalie sur la fonction mesurage de l'angle,
- « SERVICE D2 » : anomalie dans le pilotage du moteur et/ou de l'attelle,
- « SERVICE D3 » : anomalie sur le sens de rotation du moteur.

Contactez votre spécialiste KINETEC le plus proche si le problème persiste, après avoir mis hors tension, puis sous tension, puis redémarré par appui sur la touche « START/STOP ».

12- NETTOYAGE :

Avant tout, mettre hors tension l'attelle en déconnectant le cordon secteur.

Utiliser un produit de DESINFECTION (solution à base de PROPANOL/ISOPROPANOL ou à base d'ALDEHYDES) par pulvérisation des surfaces (habillages, éléments métalliques, capots plastiques).

Afin d'assurer une hygiène optimale, il est conseillé de nettoyer les habillages à chaque nouveau patient, tous les consommables de l'appareil peuvent être jetés sans danger.

13- SYMBOLES UTILISES :

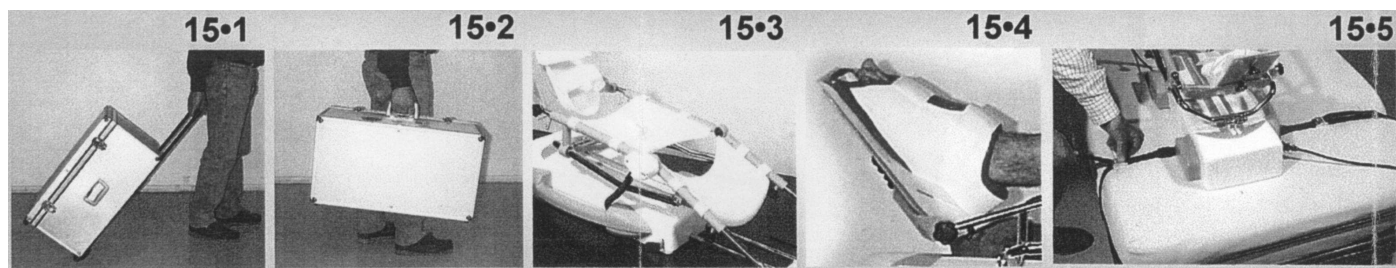
	Appareil de TYPE B (protection contre les chocs électriques)
	ATTENTION (consulter les documents d'accompagnement)
	ARRÊT (mise hors-tension)
	MARCHE (mise sous-tension)
	Platine électronique sous tension (12Vdc)

	VITESSE
	EXTENSION
	FLEXION
	Service
	Poignée de commande

14- CONDITIONS DE GARANTIES :

KINETEC garantit ses appareils de mobilisation passive articulaire 1 an contre tout vice de fabrication, à partir de la date d'achat par le consommateur.

15- ACCESSOIRES :



15-1 valise de transport avec roulettes.

15-2 valise de transport sans roulette.

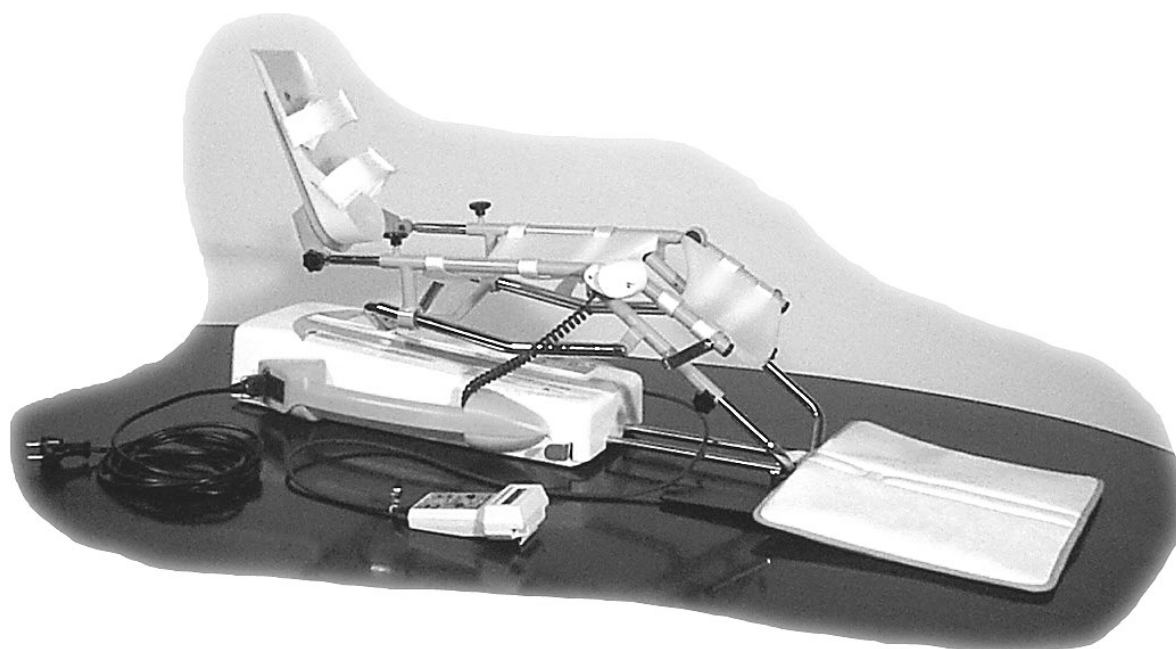
15-3 coques plastiques.

15-4 chausson.

15-5 sangles d'attache au lit.

Sciences et Technologies Industrielles
Génie Electronique

ATTELLE DE GENOU



11. DOCUMENTATION CONSTRUCTEUR :

- 12.1) LP2951ACMX : Micropower Voltage Regulator (Pages 40 à 43).
- 12.2) AFFICH1X16839555 : Afficheur LCD 1×16 caractères (Pages 44 à 48).
- 12.3) 4013 : Dual D Type Flip-Flop (Pages 49 à 52).
- 12.4) 74AC32 : Quad 2 Input OR Gate (Pages 53 à 56).
- 12.5) 74HC14 : Hex Inverter Schmitt Trigger (Pages 57 à 59).
- 12.6) 74HCT08 : Quad 2 Input AND Gate (Pages 60 à 62).
- 12.7) BAS32 : Diode 75V ; 200mA (Pages 63 à 65).
- 12.8) BC817-25 : Transistor NPN 45V 500mA (Pages 66 à 67).
- 12.9) BC337-25 : Transistor NPN 45V 500mA (équivalent BC817-25 en traversant) (Pages 68 à 69).
- 12.10) BYD17J : Diode 600V ; 1,5A (Pages 70 à 72).
- 12.11) BZV55C5V1 : Diode zener 5,1V ; 500mW (Pages 73 à 76).
- 12.12) 7660SCBA : Super voltage converter (Pages 77 à 79).
- 12.13) IRF7201 : HEXFET POWER MOSFET – N_CHANNEL (Pages 80 à 84).
- 12.14) IRF7205 : HEXFET POWER MOSFET – P_CHANNEL (Pages 85 à 89).
- 12.15) 78L05CD : Positive Voltage Regulator (Pages 90 à 92).
- 12.16) SM6T18A : “Transil” 18V ; 600W/1mS (Pages 93 à 95).
- 12.17) TL074 : Quad Fet Operational Amplifier (Pages 96 à 99).
- 12.18) TLE2062CD : Dual Operational Amplifier (Pages 100 à 105).
- 12.19) TMS370C758AFNT : Microcontrôleur 8bits TMS370 (Pages 106 à 123)
- 12.20) DS1233D10 : Moniteur de tension 5V DS123 (Pages 124 à 128).
- 12.21) QUARTZ16MHZHC49S : Quartz 16MHz HC49S (Page 129).



September 2003

LP2950/LP2951

Series of Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75µA typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950-5.0 is available in the surface-mount D-Pak package, and in the popular 3-pin TO-92 package for pin-compatibility with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strappeded for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation

(.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

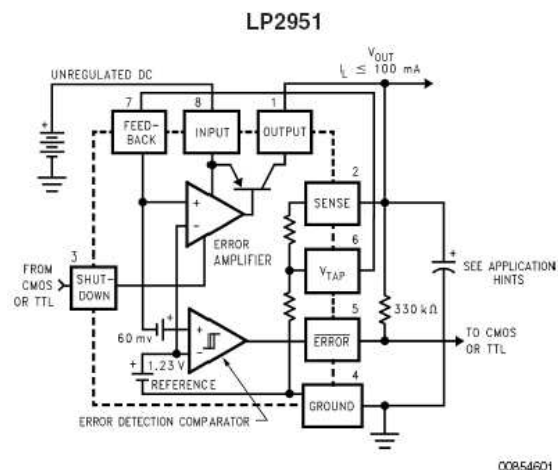
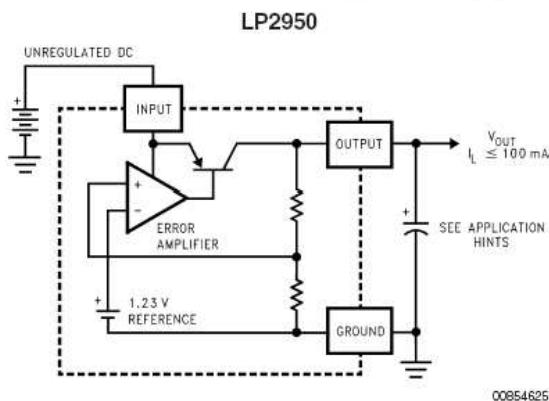
Features

- 5V, 3V, and 3.3V versions available
- High accuracy output voltage
- Guaranteed 100mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs minimum capacitance for stability
- Current and Thermal Limiting
- Stable with low-ESR output capacitors

LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

Block Diagram and Typical Applications



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Supply Voltage	-0.3 to +30V
SHUTDOWN Input Voltage, Error Comparator Output Voltage, (Note 9)	
FEEDBACK Input Voltage (Note 9) (Note 10)	-1.5 to +30V
Power Dissipation	Internally Limited
Junction Temperature (T_J)	+150°C
Ambient Storage Temperature	-65° to +150°C
Soldering Dwell Time, Temperature	
Wave	4 seconds, 260°C
Infrared	10 seconds, 240°C
Vapor Phase	75 seconds, 219°C

ESD Rating

Human Body Model(Note 18)

2500V

Operating Ratings (Note 1)

Maximum Input Supply Voltage	30V
Junction Temperature Range (T_J) (Note 8)	
LP2951	-55° to +150°C
LP2950AC-XX, LP2950C-XX, LP2951AC-XX, LP2951C-XX	-40° to +125°C

Electrical Characteristics (Note 2)

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
3V Versions (Note 17)										
Output Voltage	T _J = 25°C	3.0	3.015 2.985	3.0	3.015 2.985		3.0	3.030 2.970		V max V min
	–25°C ≤ T _J ≤ 85°C	3.0		3.0		3.030 2.970	3.0		3.045 2.955	V max V min
	Full Operating Temperature Range	3.0	3.036 2.964	3.0		3.036 2.964	3.0		3.060 2.940	V max V min
Output Voltage	100μA ≤ I _L ≤ 100mA	3.0	3.045	3.0		3.042	3.0		3.072	V max
	T _J ≤ T _{JMAX}		2.955			2.958			2.928	V min
3.3V Versions (Note 17)										
Output Voltage	T _J = 25°C	3.3	3.317 3.284	3.3	3.317 3.284		3.3	3.333 3.267		V max V min
	–25°C ≤ T _J ≤ 85°C	3.3		3.3		3.333 3.267	3.3		3.350 3.251	V max V min
	Full Operating Temperature Range	3.3	3.340 3.260	3.3		3.340 3.260	3.3		3.366 3.234	V max V min
Output Voltage	100μA ≤ I _L ≤ 100mA	3.3	3.350	3.3		3.346	3.3		3.379	V max
	T _J ≤ T _{JMAX}		3.251			3.254			3.221	V min
5V Versions (Note 17)										
Output Voltage	T _J = 25°C	5.0	5.025 4.975	5.0	5.025 4.975		5.0	5.05 4.95		V max V min
	–25°C ≤ T _J ≤ 85°C	5.0		5.0		5.05 4.95	5.0		5.075 4.925	V max V min
	Full Operating Temperature Range	5.0	5.06 4.94	5.0		5.06 4.94	5.0		5.1 4.9	V max V min
Output Voltage	100μA ≤ I _L ≤ 100mA	5.0	5.075	5.0		5.075	5.0		5.12	V max
	T _J ≤ T _{JMAX}		4.925			4.925			4.88	V min

Electrical Characteristics (Note 2) (Continued)										
Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
All Voltage Options										
Output Voltage Temperature Coefficient	(Note 12)	20	120	20		100	50		150	ppm/°C
Line Regulation (Note 14)	$(V_{O\text{NOM}} + 1)V \leq V_{in} \leq 30V$ (Note 15)	0.03	0.1 0.5	0.03	0.1	0.2	0.04	0.2	0.4	% max % max
Load Regulation (Note 14)	$100\mu A \leq I_L \leq 100mA$	0.04	0.1 0.3	0.04	0.1	0.2	0.1	0.2	0.3	% max % max
Dropout Voltage (Note 5)	$I_L = 100\mu A$		80		80			80		mV max
		50	150	50		150	50		150	mV max
	$I_L = 100mA$		450		450			450		mV max
		380	600	380		600	380		600	mV max
Ground Current	$I_L = 100\mu A$	75	120 140	75	120	140	75	120	140	μA max μA max
		8	12 14	8	12	14	8	12	14	mA max mA max
	$I_L = 100mA$									
Dropout Ground Current	$V_{in} = (V_{O\text{NOM}} - 0.5)V$ $I_L = 100\mu A$	110	170 200	110	170	200	110	170	200	μA max μA max
Current Limit	$V_{out} = 0$	160	200 220	160	200	220	160	200	220	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 kHz	$C_L = 1\mu F$ (5V Only)	430		430			430			μV rms
	$C_L = 200\mu F$	160		160			160			μV rms
	$C_L = 3.3\mu F$ (Bypass = 0.01 μF Pins 7 to 1 (LP2951))	100		100			100			μV rms
8-pin Versions Only		LP2951		LP2951AC-XX			LP2951C-XX			
Reference Voltage		1.235	1.25 1.26 1.22 1.2	1.235	1.25 1.22	1.26 1.2	1.235	1.26 1.21	1.27 1.2	V max V max V min V min
Reference Voltage	(Note 7)		1.27 1.19			1.27 1.19			1.285 1.185	V max V min
Feedback Pin Bias Current		20	40 60	20	40	60	20	40	60	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Error Comparator										
Output Leakage Current	$V_{OH} = 30V$	0.01	1 2	0.01	1	2	0.01	1	2	μA max μA max
Output Low Voltage	$V_{in} = (V_{O\text{NOM}} - 0.5)V$ $I_{OL} = 400\mu A$	150	250 400	150	250	400	150	250	400	mV max mV max

Electrical Characteristics (Note 2) (Continued)

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
Error Comparator										
Upper Threshold Voltage	(Note 6)	60	40 25	60	40	25	60	40	25	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 140	75	95	140	75	95	140	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV
Shutdown Input										
Input Logic Voltage	Low (Regulator ON) High (Regulator OFF)	1.3	0.6 2.0	1.3		0.7 2.0	1.3		0.7 2.0	V V max V min
Shutdown Pin Input Current	V _{shutdown} = 2.4V	30	50 100	30	50	100	30	50	100	µA max µA max
	V _{shutdown} = 30V	450	600 750	450	600	750	450	600	750	µA max µA max
Regulator Output Current in Shutdown	(Note 11)	3	10 20	3	10	20	3	10	20	µA max µA max

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Unless otherwise specified all limits guaranteed for $V_{\text{IN}} = (V_{\text{ONOM}} + 1)\text{V}$, $I_{\text{L}} = 100\mu\text{A}$ and $C_{\text{L}} = 1\mu\text{F}$ for 5V versions and $2.2\mu\text{F}$ for 3V and 3.3V versions. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for $T_{\text{A}} = T_{\text{J}} = 25^{\circ}\text{C}$. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP} , OUTPUT tied to SENSE, and $V_{\text{SHUTDOWN}} \leq 0.8\text{V}$.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at $V_{\text{IN}} = (V_{\text{ONOM}} + 1)\text{V}$. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain $= V_{\text{OUT}}/V_{\text{REF}} = (R1 + R2)/R2$. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by $95\text{mV} \times 5\text{V}/1.235\text{V} = 384\text{mV}$. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{\text{REF}} \leq V_{\text{OUT}} \leq (V_{\text{IN}} - 1\text{V})$, $2.3\text{V} \leq V_{\text{IN}} \leq 30\text{V}$, $100\mu\text{A} \leq I_{\text{L}} \leq 100\text{mA}$, $T_{\text{J}} \leq T_{\text{JMAX}}$.

Note 8: The junction-to-ambient thermal resistances are as follows: 180°C/W and 160°C/W for the TO-92 package with 0.40 inch and 0.25 inch leads to the printed circuit board (PCB) respectively, 105°C/W for the molded plastic DIP (N), 130°C/W for the ceramic DIP (J), 160°C/W for the molded plastic SOP (M), 200°C/W for the molded plastic MSOP (MM), and 160°C/W for the metal can package (H). The above thermal resistances for the N, J, M, and MM packages apply when the package is soldered directly to the PCB. Junction-to-case thermal resistance for the H package is 20°C/W . Junction-to-case thermal resistance for the TO-252 package is 5.4°C/W . The value of θ_{JA} for the LLP package is typically 51°C/W but is dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For details of thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{\text{shutdown}} \geq 2\text{V}$, $V_{\text{IN}} \leq 30\text{V}$, $V_{\text{OUT}} = 0$, Feedback pin tied to V_{TAP} .

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50mA load pulse at $V_{\text{IN}} = 30\text{V}$ (1.25W pulse) for $T = 10\text{ms}$.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 15: Line regulation for the LP2951 is tested at 150°C for $I_{\text{L}} = 1\text{mA}$. For $I_{\text{L}} = 100\mu\text{A}$ and $T_{\text{J}} = 125^{\circ}\text{C}$, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

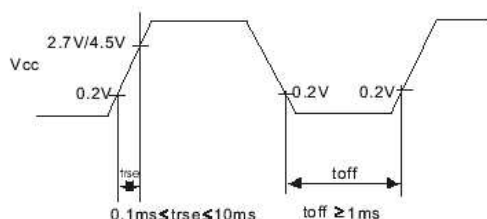
Note 16: A Military RETS specification is available on request. At time of printing, the LP2951 RETS specification complied with the boldface limits in this column. The LP2951H, WG, or J may also be procured as Standard Military Drawing Spec #5962-3870501MGA, MXA, or MPA.

Note 17: All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3.0V and 3.3V versions are designated by the last two digits, but the 5V version is denoted with no code at this location of the part number (refer to ordering information table).

Note 18: Human Body Model $1.5\text{k}\Omega$ in series with 100pF .

POWER SUPPLY RESET

The internal reset circuit will be operating properly when the following power supply conditions are satisfied. If it is not operated properly, please perform the initial setting along with the instruction.



Item	Symbol	Measuring Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Power Supply RISE Time	t_{rise}	—	0.1	—	10	mS
Power Supply CFF Time	t_{off}	—	1	—	—	mS

Reset Function

Initialization Mode by Internal Reset Circuit

The controller automatically initializes (resets) when power is supplied (built-in internal reset circuit). The following instructions are executed during initialization. The busy flag (BF) is kept in busy state until initialization ends (BF=1). The busy state is 10ms after V_{dd} reaches 4.5V.

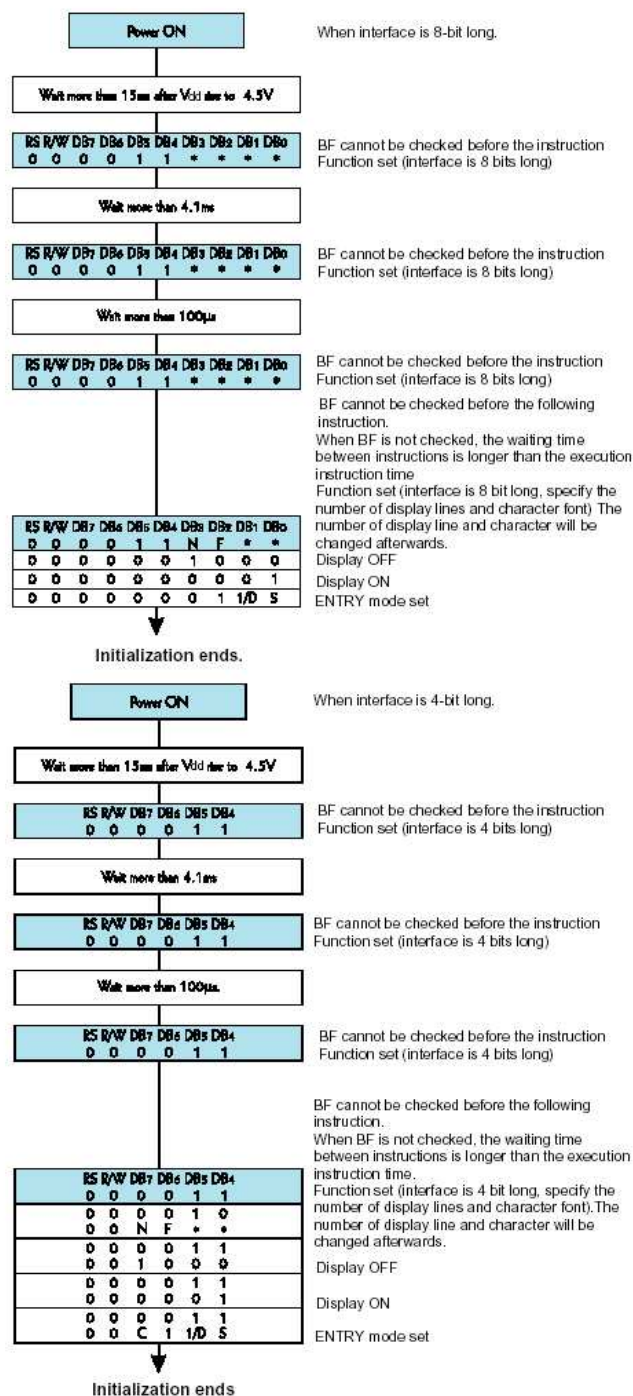
- (1) Display clear
 - DL=1: 8 bit long interface data
 - DL=0: 4 bit F=0: 5 x 7 dots character font
 - N=1: 2 lines
 - N=0: 1 line
- (2) Function set
 - D=0: Display OFF
 - C=0: Cursor OFF
 - B=0: Blink OFF
- (3) Display ON/OFF control
 - D=0: Display OFF
 - C=0: Cursor OFF
 - B=0: Blink OFF
- (4) Entry mode set
 - 1 / D = 1: + 1 (increment)
 - S = 0: No shift

Note: When using internal reset circuit is not satisfied in power supply conditions, the internal reset circuit will not function properly and initialization will not be performed. Please initialize using the MPU along with the instruction set.

Initialization along with Instruction

If power supply conditions are not satisfied, which for proper operation of internal reset circuit, it is required to make initialization along with instruction.

Please make following procedures.



ELECTRICAL CHARACTERISTICS

V_{dd} = 5V $\pm$ 5%V_{ss} = 0V

Item	Symbol	Condition	Standard value			Unit.	Applicable terminal
			Min.	Typ.	Max.		
Power voltage	V _{dd}		4.5	5.00	5.5	V	V _{dd}
Input H- level voltage	V _{IH}		2.2	—	V _{dd}	V	RS,R/ $\overline{W}$,E
Input L- level voltage	V _{IL}		-0.3	—	0.6	V	DB0~DB7
Output H- level voltage	V _{OH}	I _{OH} = 0.205mA	2.4	—	—	V	DB0~DB7
Output L- level voltage	V _{OL}	I _{OL} = 1.2mA	—	—	0.4	V	
I/O leakage current	I _{IL}	V _{in} = 0~V _{dd}	-1	—	1.0	μ A	RS,R/ $\overline{W}$,E DB0~DB7
Supply current	I _{dd}	V _{dd} = 5V	2	—	—	mA	V _{dd}
LCD operating voltage	V _{LCD}	V _{dd} - V ₀	3.0	—	11.0	V	V ₀

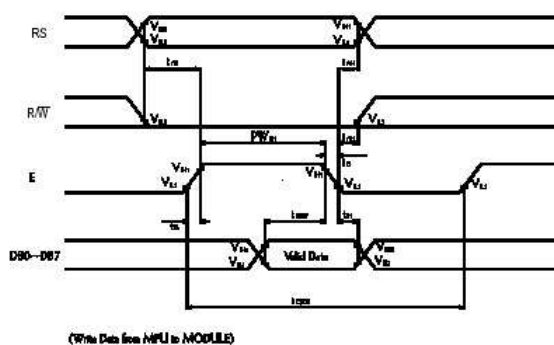
TIMING CHARACTERISTICS

V_{dd} = 5V $\pm$ 5%V_{ss} = 0V

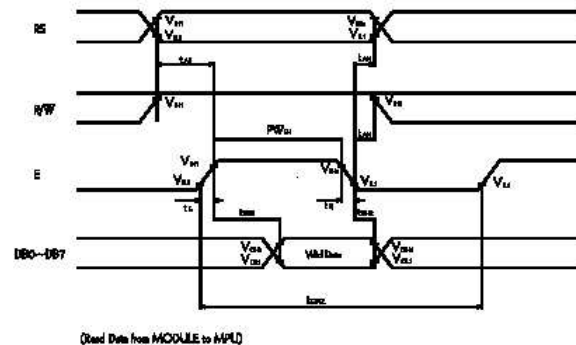
Item	Symbol	Min.	Max.	Unit.
Enable cycle time	T _{cyce}	500	—	ns
Enable pulse width	P _{WEH}	200	—	ns
Enable rise/fall time	T _{ER} , T _{EF}	—	25	ns
Set-up time	T _{AS}	40	—	ns
Address hold time	T _{AH}	10	—	ns
Data Set-up time	T _{DSH}	60	—	ns
Data delay time	T _{DDR}	60	120	ns
Data hold time (writing)	T _H	10	—	ns
Data hold time (reading)	T _{DHR}	20	—	ns
Clock oscillating frequency	T _{osc}	270(Typ.)		KHz

TIMING CHART

◆ FIG.1 WRITE OPERATION

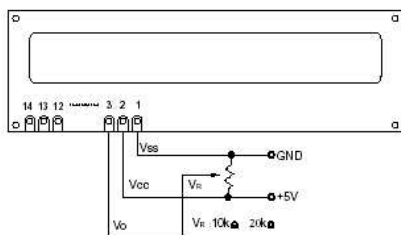


◆ FIG.2 READ OPERATION

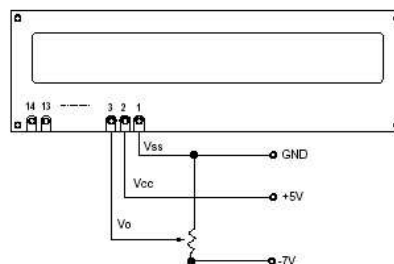


EXAMPLE OF POWER SUPPLY

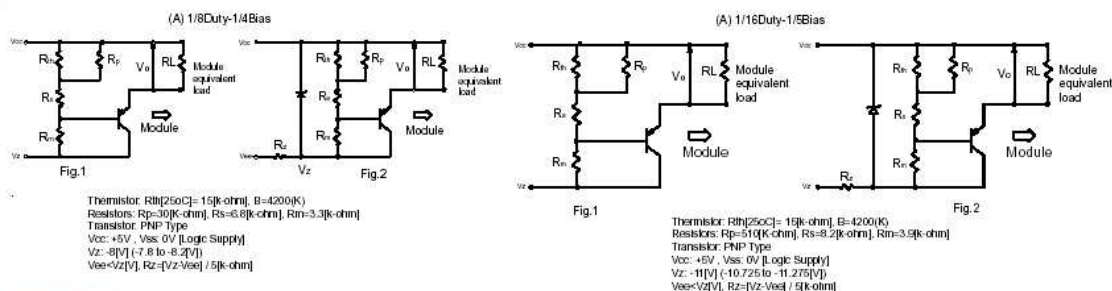
Normal Temperature Type



Extended Temperature Type



Examples of Temperature Compensation Circuits for Extended Temp. (Only for reference)



INSTRUCTIONS

Instruction	Code										Description	Executed Time(max.)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	1.64mS
Cursor Art Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home positio (Address 0). Also returns the display bing shifted to the original position. DD RAM contents remain unchanged.	1.64mS
Entry Mode Set	0	0	0	0	0	0	0	1	1/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40μS
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor NO/OFF (C), and blink of cursor position character (B).	40μS
Cursor /Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40μS
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F)	40μS
CG RAM Address Set	0	0	0	1	ACG						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40μS
DD RAM Address Set	0	0	1	ADD						Sets the DD RAM address. DD RAM data is sent and received after this setting.	40μS	
Busy Flag/ Address Read	0	1	BF	AC						Reads Busy flag (FB) indicating internal operation is being performed and reads address counter counts.	0μS	
CG RAM / DD RAM Data Write	1	0	WRITE DATA						Writes data into DD RAM or CG RAM.	40μS		
CG RAM / DD RAM Data Read	1	1	READ DATA						Reads data from DD RAM or CG RAM.	40μS		
Code											Description	Executed Time (max)
I / D = 1 : Increment I / D = 0 : Decrement S = 1 : With display shift S / C = 0 : cursor movement R / L = 1 : Shift to the right R / L = 0 : Shift to the left D L = 1 : 8-bit			D / L = 0 : 4-bit N = 1 : 2 lines N = 0 : 1 line F = 1 : 5 x 10 dots F = 0.5 x 7 dots BF = 1 : internal operation is being performed BF = 0 : instruction acceptable								DD RAM : Display Data RAM CG RAM : Character Generator RAM ACG : CG RAM Address ADD : DD RAM Address Corresponds to cursor address AC : Address Counter, used for both DD RAM and CG RAM * : Invalid	fcp or fosc = 250 KHz However, when frequency changes, eecution time also changes Example if fcp or fosc is 270KHz, 70μS x 250 / 270 = 37μS

HD44780U**Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)**

	Lower 4 Bits	Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
xxxx0000		CG RAM (1)				0	@	P	`	P				-	9	3	α	p	
xxxx0001	(2)				!	1	A	Q	a	q				。	7	チ	△	ä	q
xxxx0010	(3)				"	2	B	R	b	r				「	イ	ツ	×	β	θ
xxxx0011	(4)				#	3	C	S	c	s				」	ウ	テ	ε	ε	ω
xxxx0100	(5)				\$	4	D	T	d	t				、	エ	ト	ト	μ	Ω
xxxx0101	(6)				%	5	E	U	e	u				・	オ	ナ	1	℃	Ü
xxxx0110	(7)				&	6	F	V	f	v				ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)				'	7	G	W	g	w				ア	キ	ヌ	ウ	g	π
xxxx1000	(1)				<	8	H	X	h	x				ィ	ク	ネ	リ	フ	×
xxxx1001	(2)				>	9	I	Y	i	y				ウ	ケ	ル	ル	´	y
xxxx1010	(3)				*	:	J	Z	j	z				エ	コ	ハ	レ	j	チ
xxxx1011	(4)				+	;	K	[	k	{				オ	サ	ヒ	ロ	*	斤
xxxx1100	(5)				,	<	L	¥	l	l				カ	シ	フ	ワ	Φ	円
xxxx1101	(6)				-	=	M	]	m	}				ユ	ズ	ハ	ン	も	÷
xxxx1110	(7)				.	>	N	^	n	÷				ヨ	セ	ホ	ハ	ん	
xxxx1111	(8)				/	?	O	_	o	€				ッ	ソ	マ	°	ö	■

Note: The user can specify any pattern for character-generator RAM.

HD44780U

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A02)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)	▶		0	Q	P	`	P	E	α		°	À	0	À	Σ
xxxx0001	(2)	◀	!	1	A	Q	a	q	A	J	i	±	Á	Ñ	á	ñ
xxxx0010	(3)	“	”	2	B	R	b	r	W	Γ	φ	²	Â	Ò	â	ò
xxxx0011	(4)	”	#	3	C	S	c	s	3	π	ℓ	³	Ã	Ó	ã	ó
xxxx0100	(5)	▲	\$	4	D	T	d	t	H	Σ	x	¼	Ä	Ô	ä	ô
xxxx0101	(6)	▼	%	5	E	U	e	u	Ï	σ	¥	½	Å	Ö	å	ö
xxxx0110	(7)	◆	&	6	F	V	f	v	J	¶	!	¾	Æ	Ö	æ	ö
xxxx0111	(8)	♣	'	7	G	W	g	w	Π	τ	§	•	Ç	×	ç	÷
xxxx1000	(1)	↑	(	8	H	X	h	x	Y	*	†	ω	È	⊗	è	⊗
xxxx1001	(2)	↓	)	9	I	Y	i	y	U	θ	¹	¹	É	Ù	é	ù
xxxx1010	(3)	→	*	:	J	Z	j	z	4	Ω	³	³	Ê	Ú	ê	ú
xxxx1011	(4)	←	+	;	K	[	k	[	W	δ	«	»	Ë	Û	ë	û
xxxx1100	(5)	≤	,	<	L	\	l		W	∞	H	¼	Ì	Ü	ì	ü
xxxx1101	(6)	≥	-	=	M	]	m	}	b	⊙	Я	½	Í	Ý	í	ý
xxxx1110	(7)	▲	.	>	N	^	n	~	b	ε	Q	¾	Î	ß	î	ß
xxxx1111	(8)	▼	/	?	O	_	o	ˆ	Q	∩	‘	¿	Ï	ß	ï	ÿ

MOTOROLA
 SEMICONDUCTOR TECHNICAL DATA

MC14011B/12B (see pg 6-5)
MC14011UB/12UB (see pg 6-14)
MC14013B

Dual Type D Flip-Flop

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\bar{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	- 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

TRUTH TABLE

Inputs				Outputs	
Clock†	Data	Reset	Set	Q	$\bar{Q}$
↗	0	0	0	0	1
↗	1	0	0	1	0
↘	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = Don't Care

† = Level Change

No
Change



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646

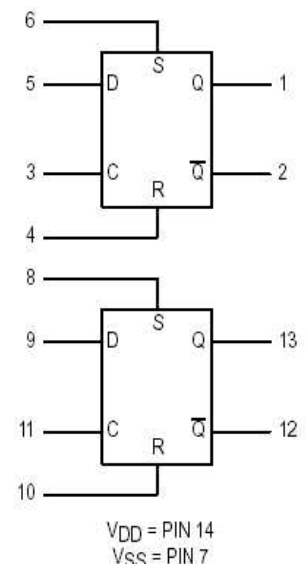


D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = - 55° to 125°C for all packages.

BLOCK DIAGRAM


ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD} "1" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
		5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) "1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Source I_{OH}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	— — — —	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	— — — —	- 1.7 - 0.36 - 0.9 - 2.4	— — — —	mAdc
	Sink I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	1.0 2.0 4.0	— — —	0.002 0.004 0.006	1.0 2.0 4.0	— — —	30 60 120	μ Adc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0 10 15	$I_T = (0.75 \mu A/kHz) f + I_{DD}$ $I_T = (1.5 \mu A/kHz) f + I_{DD}$ $I_T = (2.3 \mu A/kHz) f + I_{DD}$							μ Adc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

** The formulas given are for the typical characteristics only at 25°C.

† To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

Q_A	1	14	V_{DD}
$\bar{Q}_A$	2	13	Q_B
C_A	3	12	$\bar{Q}_B$
R_A	4	11	C_B
D_A	5	10	R_B
S_A	6	9	D_B
V_{SS}	7	8	S_B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
		15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I _{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc	
		10	—	2.0	—	0.004	2.0	—	60		
		15	—	4.0	—	0.006	4.0	—	120		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.75 μA/kHz) f + I _{DD} I _T = (1.5 μA/kHz) f + I _{DD} I _T = (2.3 μA/kHz) f + I _{DD}							μAdc	
		10									
		15									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

Q_A	1	14	V_{DD}
$\bar{Q}_A$	2	13	Q_B
C_A	3	12	$\bar{Q}_B$
R_A	4	11	C_B
D_A	5	10	R_B
S_A	6	9	D_B
V_{SS}	7	8	S_B

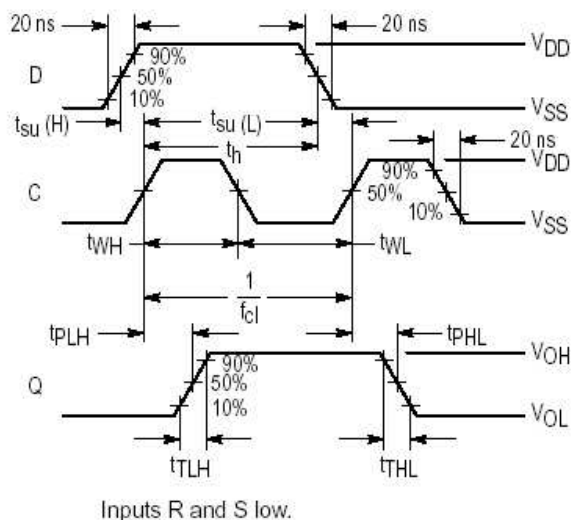


Figure 1. Dynamic Signal Waveforms (Data, Clock, and Output)

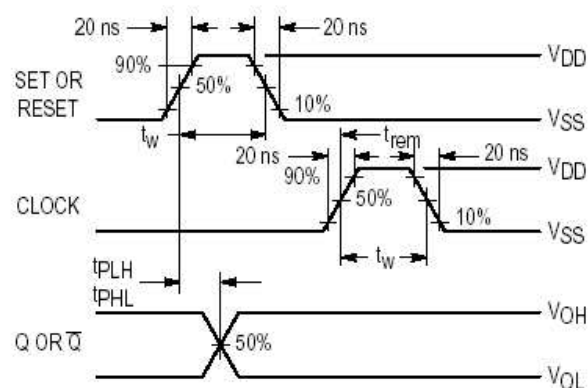
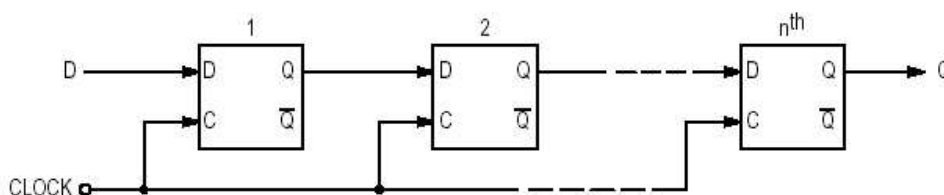


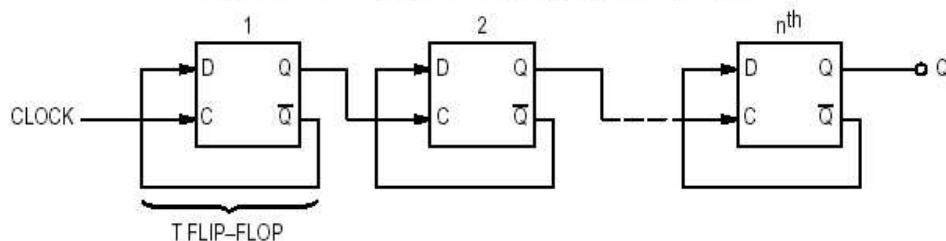
Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)

TYPICAL APPLICATIONS

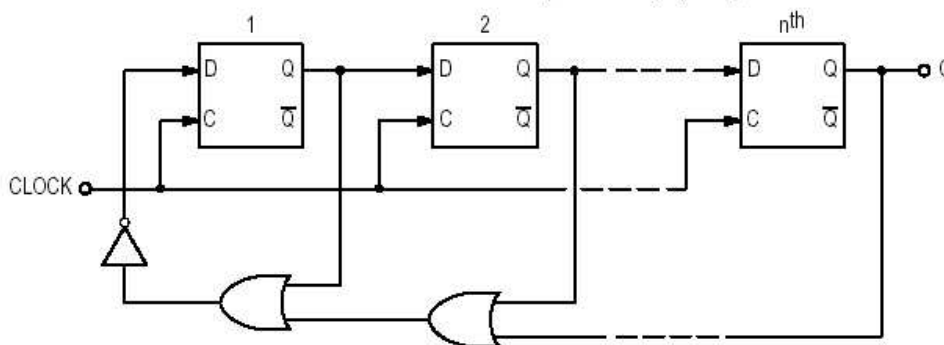
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by- 2^n)



MODIFIED RING COUNTER (Divide-by-(n+1))





March 1993

54AC/74AC32 • 74ACT32 Quad 2-Input OR Gate

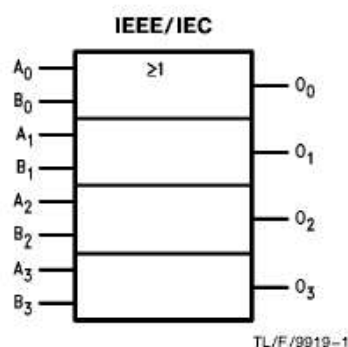
General Description

The 'AC/'ACT32 contains four, 2-input OR gates.

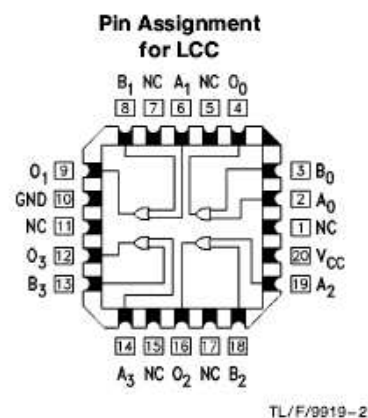
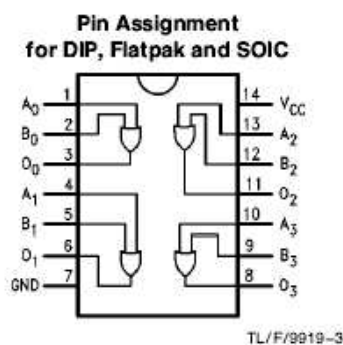
Features

- I_{CC} reduced by 50% on 54AC/74AC only
- Outputs source/sink 24 mA
- 'ACT32 has TTL-compatible inputs
- Standard Military Drawing (SMD)
— 'AC32: 5962-87614
- For Military 54ACT32, see the 54ACTQ32

Logic Symbol



Connection Diagrams



Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

FACT™ is a trademark of National Semiconductor Corporation.

54AC/74AC32 • 74ACT32 Quad 2-Input OR Gate

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.7	3.76		
		5.5		4.86	4.7	4.76		
		5.5		4.86	4.7	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.5	0.44		
		5.5		0.36	0.5	0.44		
		5.5		0.36	0.5	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	V _I = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
I _{OLD}	† Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		2.0	40.0	20.0	μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.**DC Characteristics for 'ACT Family Devices**

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{CC1}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1V
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = +25°C C _L = 50 pF			T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	7.0 5.5	9.0 7.5	1.0 1.5	12.0 9.0	1.5 1.0	10.0 8.5	ns
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	7.0 5.0	8.5 7.0	1.0 1.5	11.5 8.5	1.0 1.0	9.0 7.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t _{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns

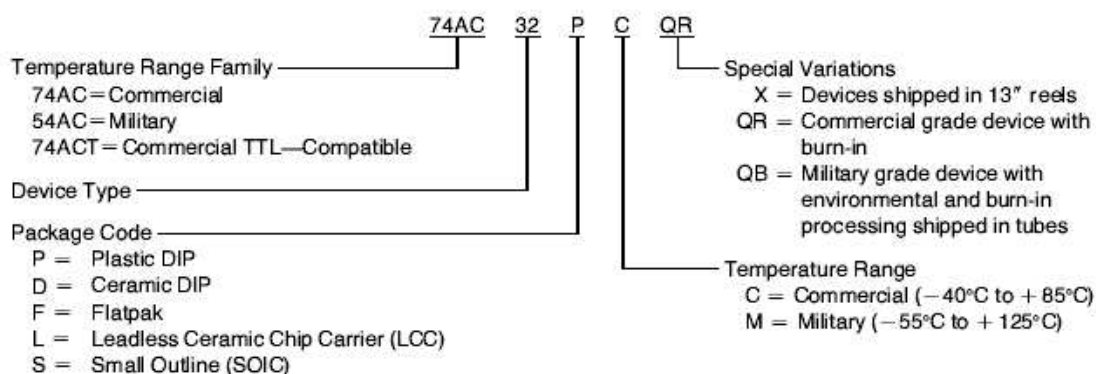
*Voltage Range 5.0 is 5.0V ± 0.3V

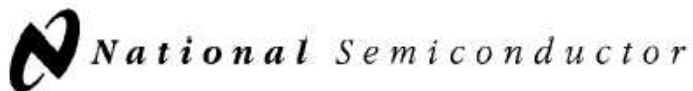
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	20.0	pF	V _{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:





November 1995

MM54HC14/MM74HC14 Hex Inverting Schmitt Trigger

General Description

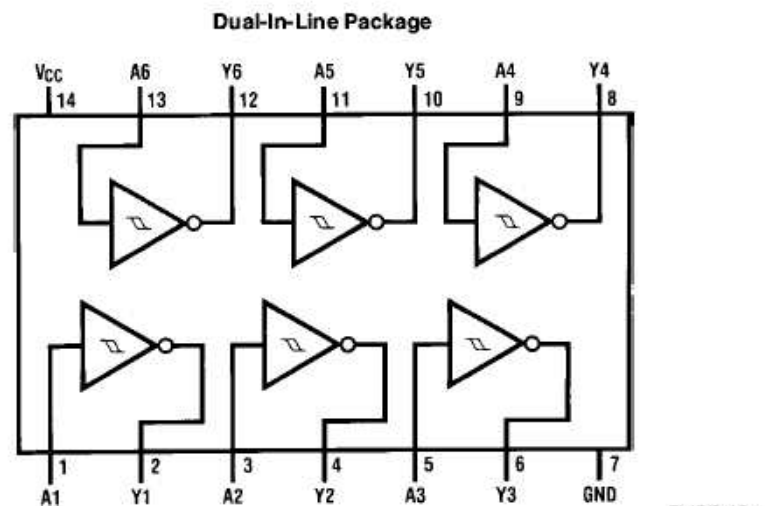
The MM54HC14/MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

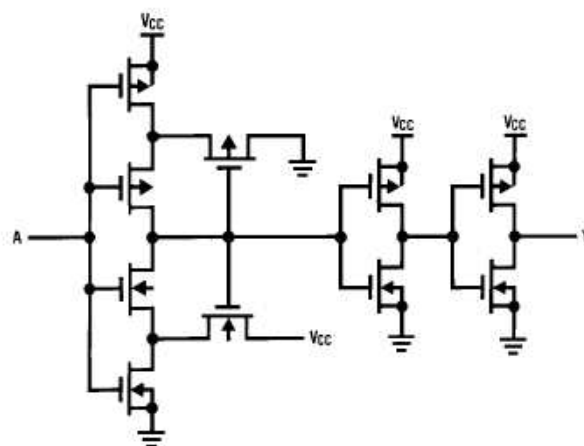
Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC} = 4.5V$

Connection and Schematic Diagrams



Order Number MM54HC14 or MM74HC14



MM54HC14/MM74HC14 Hex Inverting Schmitt Trigger

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	−0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Power Dissipation (P_D)
(Note 3)

S.O. Package only

Lead Temp. (T_L) (Soldering 10 seconds)

600 mW

500 mW

260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		74HC T _A = −40 to 85°C		54HC T _A = −55 to 125°C		Units
				Typ	Guaranteed Limits					
V _{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	1.0	V		
			4.5V	2.7	2.0	2.0	2.0	V		
			6.0V	3.2	3.0	3.0	3.0	V		
		Maximum	2.0V	1.2	1.5	1.5	1.5	V		
			4.5V	2.7	3.15	3.15	3.15	V		
			6.0V	3.2	4.2	4.2	4.2	V		
V _{T−}	Minimum	2.0V	0.7	0.3	0.3	0.3	V			
		4.5V	1.8	0.9	0.9	0.9	V			
		6.0V	2.2	1.2	1.2	1.2	V			
	Maximum	2.0V	0.7	1.0	1.0	1.0	V			
		4.5V	1.8	2.2	2.2	2.2	V			
		6.0V	2.2	3.0	3.0	3.0	V			
V _H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	0.2	V		
			4.5V	0.9	0.4	0.4	0.4	V		
			6.0V	1.0	0.5	0.5	0.5	V		
		Maximum	2.0V	0.5	1.0	1.0	1.0	V		
			4.5V	0.9	1.4	1.4	1.4	V		
			6.0V	1.0	1.5	1.5	1.5	V		
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IL} I _{OUT} = 20 μA	2.0V	2.0	1.9	1.9	1.9	V		
			4.5V	4.5	4.4	4.4	4.4	V		
			6.0V	6.0	5.9	5.9	5.9	V		
		V _{IN} = V _{IL} I _{OUT} = 4.0 mA I _{OUT} = 5.2 mA	4.5V	4.2	3.98	3.84	3.7	V		
			6.0V	5.7	5.48	5.34	5.2	V		
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} I _{OUT} = 20 μA	2.0V	0	0.1	0.1	0.1	V		
			4.5V	0	0.1	0.1	0.1	V		
			6.0V	0	0.1	0.1	0.1	V		
		V _{IN} = V _{IH} I _{OUT} = 4.0 mA I _{OUT} = 5.2 mA	4.5V	0.2	0.26	0.33	0.4	V		
			6.0V	0.2	0.26	0.33	0.4	V		
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA		
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		2.0	20	40	μA		

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

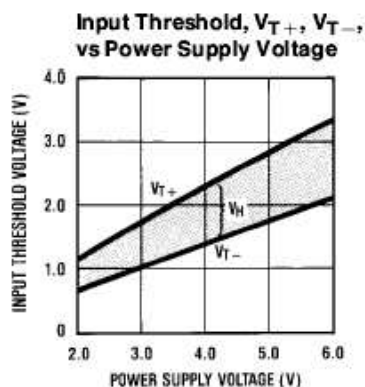
AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay		12	22	ns

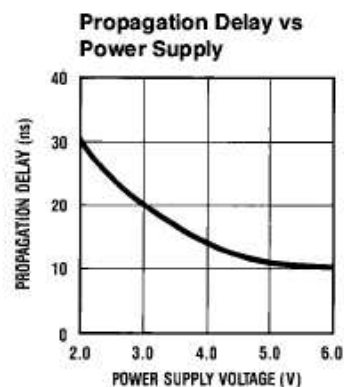
AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		74HC T _A = − 40 to 85°C	54HC T _A = − 55 to 125°C	Units
				Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	60	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	11	21	26	32	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

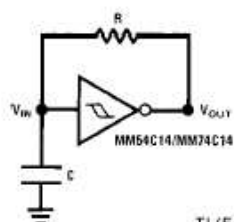
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Performance Characteristics

TL/F/5105-3



TL/F/5105-4

Typical Applications**Low Power Oscillator**

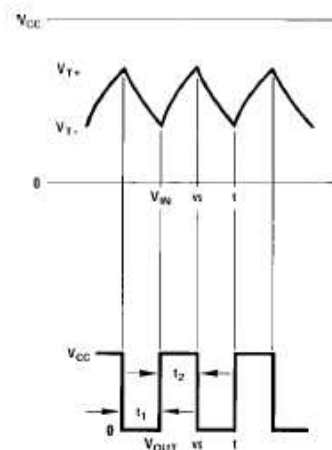
TL/F/5105-5

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

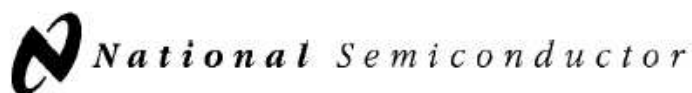
$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$

Note: The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$



TL/F/5105-6



January 1988

MM54HCT08/MM74HCT08 Quad 2-Input AND Gate

General Description

The MM54HCT08/MM74HCT08 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

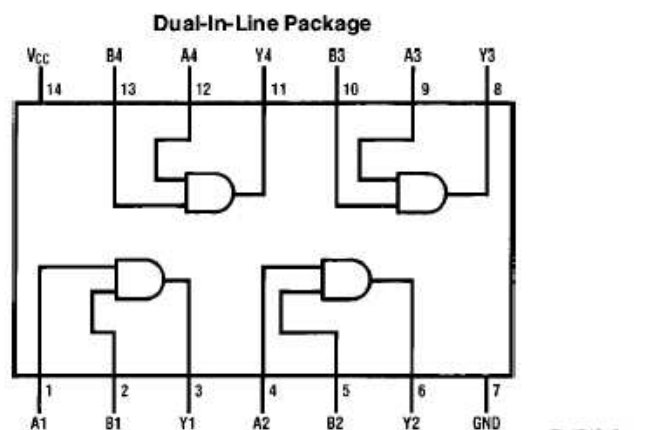
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS

devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

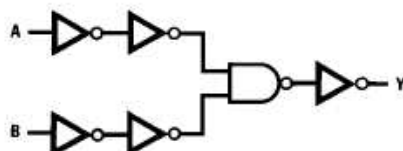
Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH} , t_{PHL} = 12 ns (typ)
- Low power: 10 μ W at DC
- High fan-out, 10 LS-TTL loads

Connection and Logic Diagrams



Order Number MM54HCT08 or MM74HCT08



MM54HCT08/MM74HCT08 Quad 2-Input AND Gate

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	−0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC}=5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		74HCT T _A = −40 to 85°C	54HCT T _A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V _{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					
		I _{OUT} = 20 μA	V _{CC}	V _{CC} − 0.1	V _{CC} − 0.1	V _{CC} − 0.1	V
		I _{OUT} = 4.0 mA, V _{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		I _{OUT} = 4.8 mA, V _{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V _{OL}	Maximum Low Level Voltage	V _{IN} = V _{IH}					
		I _{OUT} = 20 μA	0	0.1	0.1	0.1	V
		I _{OUT} = 4.0 mA, V _{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		I _{OUT} = 4.8 mA, V _{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND		2.0	20	40	μA
		I _{OUT} = 0 μA					
		V _{IN} = 2.4V or 0.5V (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package — 12 mW/°C from 65°C to 85°C; ceramic "J" package 12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC} = 5.0V$, $t_r = t_f = 6\text{ ns}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH} , t_{PHL}	Maximum Propagation Delay		9	15	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6\text{ ns}$, $C_L = 50\text{ pF}$

Symbol	Parameter	Conditions	T _A = 25°C		74HCT T _A = −40 to 85°C	54HCT T _A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
t _{PLH} , t _{PHL}	Maximum Propagation Delay		11	18	23	27	ns
t _{THL} , t _{TLH}	Maximum Output Rise & Fall Time		7	15	19	22	ns
C _{PD}	Power Dissipation Capacitance	(Note 5)	38				pF
C _{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption. $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ and the no load dynamic current consumption. $I_S = C_{PD} V_{CC} f + I_{CC}$.

General purpose diode

BAS321

FEATURES

- Small plastic SMD package
- Switching speed: max. 50 ns
- General application
- Continuous reverse voltage: max. 200 V
- Repetitive peak reverse voltage: max. 250 V
- Repetitive peak forward current: max. 625 mA.

APPLICATIONS

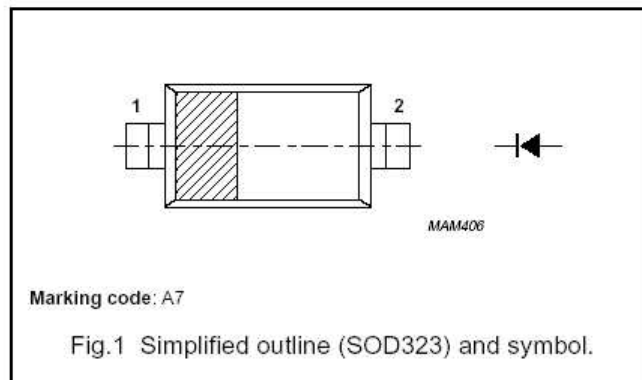
- General purpose switching in e.g. surface mounted circuits.

DESCRIPTION

The BAS321 is a general purpose diode fabricated in planar technology and encapsulated in a plastic SOD323 package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	250	V
V_R	continuous reverse voltage		–	200	V
I_F	continuous forward current	see Fig. 2; note 1	–	250	mA
I_{FRM}	repetitive peak forward current	$t_p < 0.5$ ms; $\delta \leq 0.25$	–	625	mA
I_{FSM}	non-repetitive peak forward current	square wave; $T_j = 25$ °C prior to surge; see Fig. 4			
		$t = 1$ μ s	–	9	A
		$t = 100$ μ s	–	3	A
		$t = 10$ ms	–	1.7	A
P_{tot}	total power dissipation	$T_{amb} = 25$ °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed circuit-board.

General purpose diode

BAS321

ELECTRICAL CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	see Fig. 3 $I_F = 100\text{ mA}$ $I_F = 200\text{ mA}$	1 1.25	V V
I_R	reverse current	see Fig. 5 $V_R = 200\text{ V}$ $V_R = 200\text{ V}; T_j = 150\text{ }^{\circ}\text{C}$	100 100	nA μA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0$; see Fig. 6	2	pF
t_{rr}	reverse recovery time	when switched from $I_F = 30\text{ mA}$ to $I_R = 30\text{ mA}; R_L = 100\text{ }\Omega$; measured at $I_R = 3\text{ mA}$; see Fig.8	50	ns

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	$T_s = 90^{\circ}\text{C}$; note 1	130	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 2	366	K/W

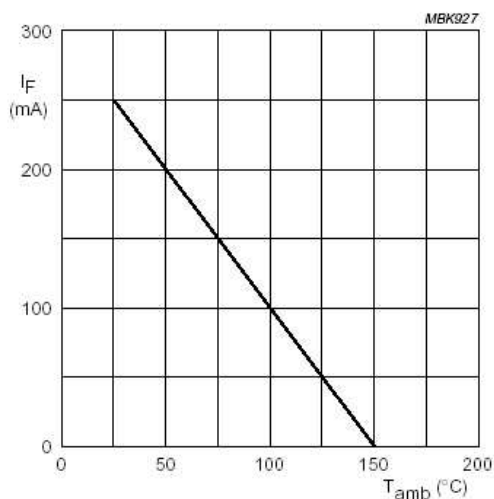
Notes

1. Soldering point of cathode tab.
2. Device mounted on an FR4 printed circuit board.

General purpose diode

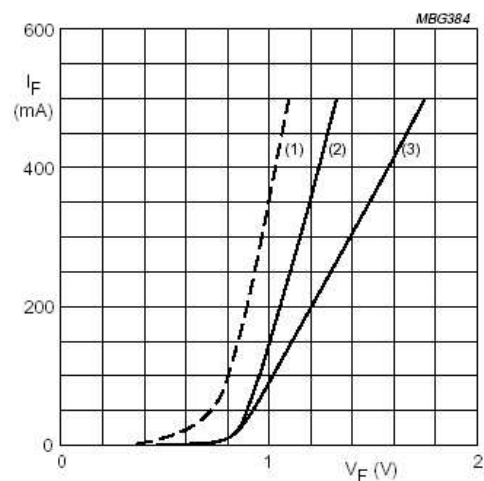
BAS321

GRAPHICAL DATA



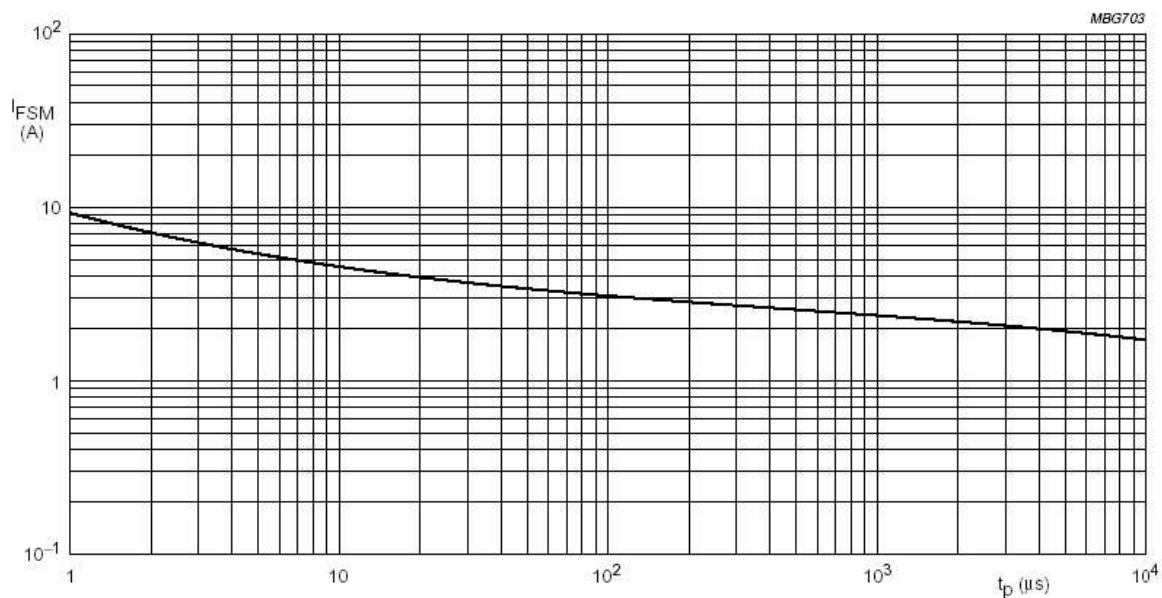
Device mounted on an FR4 printed-circuit board.

Fig.2 Maximum permissible continuous forward current as a function of ambient temperature.



- (1) $T_J = 150$ °C; typical values.
 (2) $T_J = 25$ °C; typical values.
 (3) $T_J = 25$ °C; maximum values.

Fig.3 Forward current as a function of forward voltage.

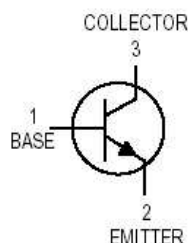
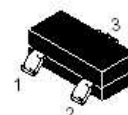


Based on square wave currents.
 $T_J = 25$ °C prior to surge.

Fig.4 Maximum permissible non-repetitive peak forward current as a function of pulse duration.

MOTOROLA
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 CASE 318-08, STYLE 6
 SOT-23 (TO-236AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	45	V
Collector-Base Voltage	V_{CBO}	50	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current — Continuous	I_C	500	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (1) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ\text{C/W}$
Total Device Dissipation Alumina Substrate, (2) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ\text{C/W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

DEVICE MARKING

BC817-16LT1 = 6A; BC817-25LT1 = 6B; BC817-40LT1 = 6C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = -10\text{ mA}$)	$V_{(BR)CEO}$	45	—	—	V
Collector-Emitter Breakdown Voltage ($V_{EB} = 0, I_C = -10\text{ }\mu\text{A}$)	$V_{(BR)CES}$	50	—	—	V
Emitter-Base Breakdown Voltage ($I_E = -1.0\text{ }\mu\text{A}$)	$V_{(BR)EBO}$	5.0	—	—	V
Collector Cutoff Current ($V_{CB} = 20\text{ V}$) ($V_{CB} = 20\text{ V}, T_A = 150^\circ\text{C}$)	I_{CBO}	— —	— —	100 5.0	nA μA

1. FR-5 = 1.0 x 0.75 x 0.062 in.

2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

Thermal Clad is a registered trademark of the Bergquist Company.

BC817-16LT1 BC817-25LT1 BC817-40LT1**ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain ($I_C = 100\text{ mA}$, $V_{CE} = 1.0\text{ V}$) ($I_C = 500\text{ mA}$, $V_{CE} = 1.0\text{ V}$)	h_{FE}	100 160 250 40	— — — —	250 400 600 —	—
Collector–Emitter Saturation Voltage ($I_C = 500\text{ mA}$, $I_B = 50\text{ mA}$)	$V_{CE(sat)}$	—	—	0.7	V
Base–Emitter On Voltage ($I_C = 500\text{ mA}$, $V_{CE} = 1.0\text{ V}$)	$V_{BE(on)}$	—	—	1.2	V
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product ($I_C = 10\text{ mA}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	100	—	—	MHz
Output Capacitance ($V_{CB} = 10\text{ V}$, $f = 1.0\text{ MHz}$)	C_{obo}	—	10	—	pF

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C , one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{556^\circ\text{C/W}} = 225\text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C .
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

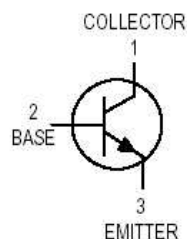
MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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Amplifier Transistors

NPN Silicon

BC337,-16,-25,-40
BC338,-16,-25,-40



CASE 29-04, STYLE 17
TO-92 (TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	BC337	BC338	Unit
Collector-Emitter Voltage	V_{CEO}	45	25	Vdc
Collector-Base Voltage	V_{CBO}	50	30	Vdc
Emitter-Base Voltage	V_{EBO}	5.0		Vdc
Collector Current — Continuous	I_C	800		mA dc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625	5.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5	12	Watt mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = 10\text{ mA}, I_E = 0$)	BC337 BC338	$V_{(BR)CEO}$	45 25	— —	— —	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 100\text{ }\mu\text{A}, I_E = 0$)	BC337 BC338	$V_{(BR)CES}$	50 30	— —	— —	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{A}, I_C = 0$)		$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 30\text{ V}, I_E = 0$) ($V_{CB} = 20\text{ V}, I_E = 0$)	BC337 BC338	I_{CBO}	— —	— —	100 100	nA dc
Collector Cutoff Current ($V_{CE} = 45\text{ V}, V_{BE} = 0$) ($V_{CE} = 25\text{ V}, V_{BE} = 0$)	BC337 BC338	I_{CES}	— —	— —	100 100	nA dc
Emitter Cutoff Current ($V_{EB} = 4.0\text{ V}, I_C = 0$)		I_{EBO}	—	—	100	nA dc

BC337,-16,-25,-40 BC338,-16,-25,-40

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain ($I_C = 100\text{ mA}$, $V_{CE} = 1.0\text{ V}$) BC337/BC338 BC337-16/BC338-16 BC337-25/BC338-25 BC337-40/BC338-40 ($I_C = 300\text{ mA}$, $V_{CE} = 1.0\text{ V}$)	h_{FE}	100 100 160 250 60	— — — — —	630 250 400 630 —	—
Base-Emitter On Voltage ($I_C = 300\text{ mA}$, $V_{CE} = 1.0\text{ V}$)	$V_{BE(on)}$	—	—	1.2	Vdc
Collector-Emitter Saturation Voltage ($I_C = 500\text{ mA}$, $I_B = 50\text{ mA}$)	$V_{CE(sat)}$	—	—	0.7	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10\text{ V}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{ob}	—	15	—	pF
Current-Gain — Bandwidth Product ($I_C = 10\text{ mA}$, $V_{CE} = 5.0\text{ V}$, $f = 100\text{ MHz}$)	f_T	—	210	—	MHz

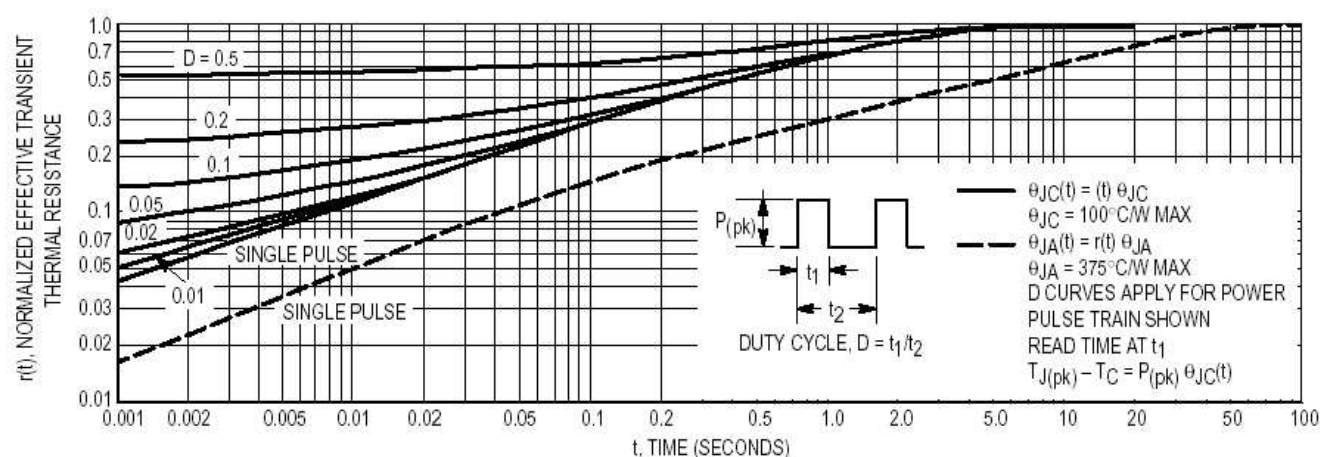


Figure 1. Thermal Response

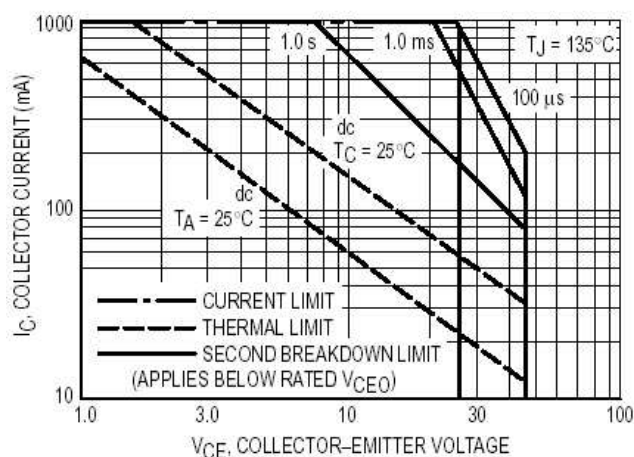


Figure 2. Active Region — Safe Operating Area

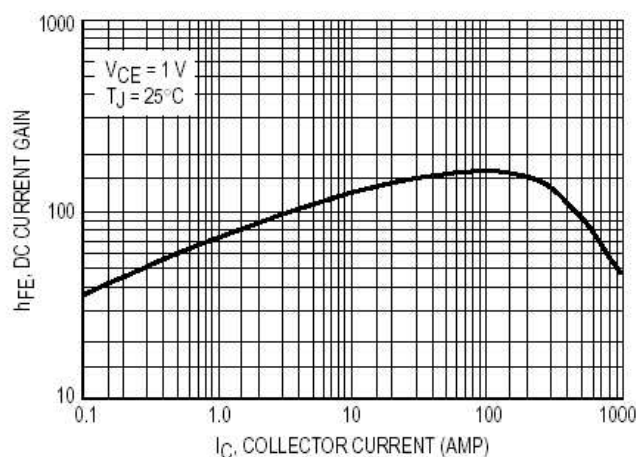


Figure 3. DC Current Gain

General purpose controlled avalanche rectifiers

BYD17 series

FEATURES

- Glass passivated
- High maximum operating temperature
- Low leakage current
- Excellent stability
- Guaranteed avalanche energy absorption capability
- Shipped in 8 mm embossed tape
- Smallest surface mount rectifier outline.

DESCRIPTION

Cavity free cylindrical glass package through Implotec™⁽¹⁾ technology.

This package is hermetically sealed and fatigue free as coefficients of expansion of all used parts are matched.

(1) Implotec is a trademark of Philips.

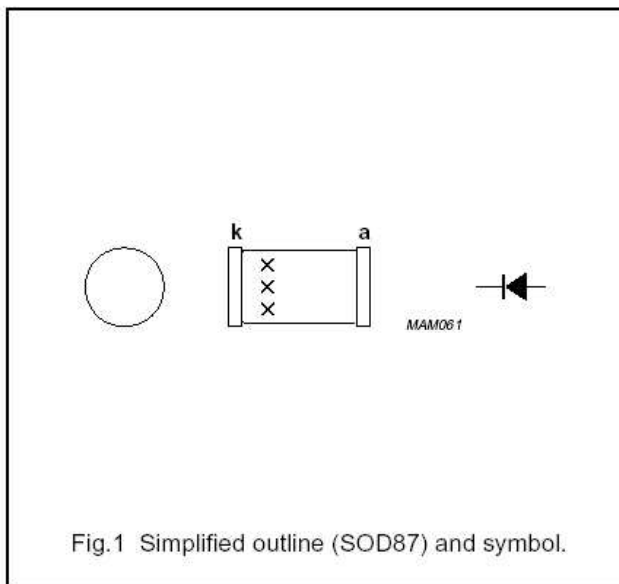


Fig.1 Simplified outline (SOD87) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage				
	BYD17D		–	200	V
	BYD17G		–	400	V
	BYD17J		–	600	V
	BYD17K		–	800	V
	BYD17M		–	1000	V
V_{RWM}	crest working reverse voltage				
	BYD17D		–	200	V
	BYD17G		–	400	V
	BYD17J		–	600	V
	BYD17K		–	800	V
	BYD17M		–	1000	V
V_R	continuous reverse voltage				
	BYD17D		–	200	V
	BYD17G		–	400	V
	BYD17J		–	600	V
	BYD17K		–	800	V
	BYD17M		–	1000	V

General purpose
controlled avalanche rectifiers

BYD17 series

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{F(AV)}$	average forward current	$T_{tp} = 105\text{ }^{\circ}\text{C}$; averaged over any 20 ms period; see Figs 2 and 4	–	1.5	A
		$T_{amb} = 65\text{ }^{\circ}\text{C}$; PCB mounting (see Fig.9); averaged over any 20 ms period; see Figs 3 and 4	–	0.6	A
I_{FSM}	non-repetitive peak forward current	$t = 10\text{ ms}$ half sinewave; $T_j = T_{j\text{ max}}$ prior to surge; $V_R = V_{RRMmax}$	–	20	A
E_{RSM}	non-repetitive peak reverse avalanche energy	$L = 120\text{ mH}$; $T_j = T_{j\text{ max}}$ prior to surge; inductive load switched off	–	7	mJ
T_{stg}	storage temperature		–65	+175	$^{\circ}\text{C}$
T_j	junction temperature	see Fig.5	–65	+175	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

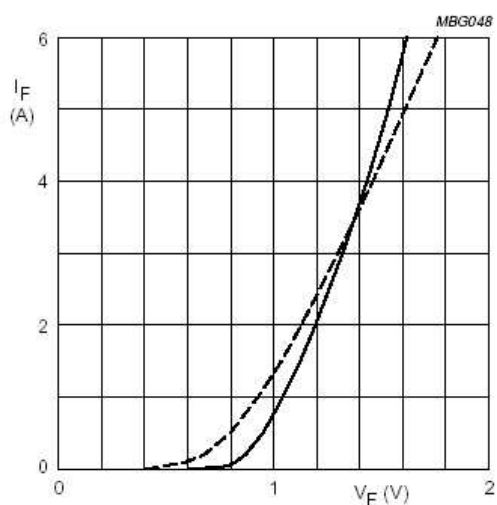
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_F	forward voltage	$I_F = 1\text{ A}$; $T_j = T_{j\text{ max}}$; see Fig.6	–	–	0.93	V
		$I_F = 1\text{ A}$; see Fig.6	–	–	1.05	V
$V_{(BR)R}$	reverse avalanche breakdown voltage	$I_R = 0.1\text{ mA}$				
			225	–	–	V
			450	–	–	V
			650	–	–	V
			900	–	–	V
			1100	–	–	V
I_R	reverse current	$V_R = V_{RRMmax}$; see Fig.7	–	–	1	μA
		$V_R = V_{RRMmax}$; $T_j = 165\text{ }^{\circ}\text{C}$; see Fig.7	–	–	100	μA
t_{rr}	reverse recovery time	when switched from $I_F = 0.5\text{ A}$ to $I_R = 1\text{ A}$; measured at $I_R = 0.25\text{ A}$; see Fig.10	–	3	–	μs
C_d	diode capacitance	$V_R = 0\text{ V}$; $f = 1\text{ MHz}$; see Fig.8	–	21	–	pF

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R_{thj-tp}	thermal resistance from junction to tie-point		30	K/W
R_{thj-a}	thermal resistance from junction to ambient	note 1	150	K/W

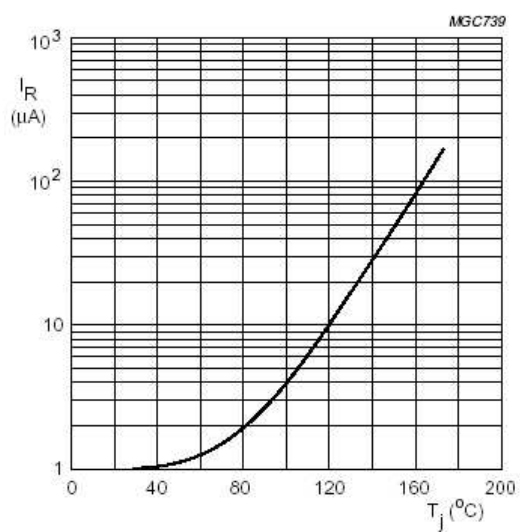
Note

1. Device mounted on epoxy-glass printed-circuit board, 1.5 mm thick; thickness of copper $\geq 40\text{ }\mu\text{m}$, see Fig.9.
For more information please refer to the "General Part of associated Handbook".



Solid line: $T_j = 25^\circ\text{C}$.
Dotted line: $T_j = 175^\circ\text{C}$.

Fig.6 Forward current as a function of forward voltage; maximum values.



$V_R = V_{RRMmax}$.

Fig.7 Reverse current as a function of junction temperature; maximum values.

Voltage regulator diodes

BZV55 series

FEATURES

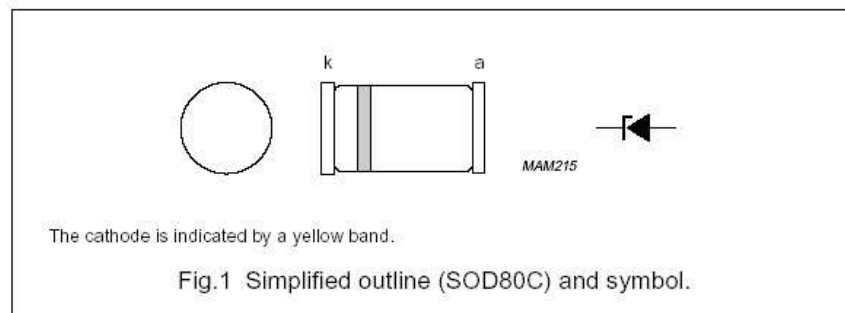
- Total power dissipation:
max. 500 mW
- Three tolerance series: $\pm 2\%$, $\pm 3\%$
and $\pm 5\%$
- Working voltage range:
nom. 2.4 to 75 V (E24 range)
- Non-repetitive peak reverse power
dissipation: max. 40 W.

APPLICATIONS

- Low-power voltage stabilizers or
voltage references.

DESCRIPTION

Low-power voltage regulator diodes in small hermetically sealed glass SOD80C SMD packages. The diodes are available in the normalized E24 $\pm 2\%$ (BZV55-B), $\pm 3\%$ (BZV55-F) and $\pm 5\%$ (BZV55-C) tolerance range. The series consists of 37 types with nominal working voltages from 2.4 to 75 V.



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_F	continuous forward current		–	250	mA
I_{ZSM}	non-repetitive peak reverse current	$t_p = 100 \mu s$; square wave; $T_j = 25^\circ C$ prior to surge	see Tables 1 and 2		
P_{tot}	total power dissipation	$T_{amb} \leq 50^\circ C$; note 1	–	400	mW
		tie-point $\leq 50^\circ C$; note 1	–	500	mW
P_{ZSM}	non-repetitive peak reverse power dissipation	$t_p = 100 \mu s$; square wave; $T_j = 25^\circ C$ prior to surge; see Fig.3	–	40	W
T_{stg}	storage temperature		–65	+200	$^\circ C$
T_j	junction temperature		–65	+200	$^\circ C$

Note

1. Device mounted on a ceramic substrate of $10 \times 10 \times 0.6$ mm.

Voltage regulator diodes

BZV55 series

ELECTRICAL CHARACTERISTICS

Total BZV55-B, F and C series

 $T_J = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_F	forward voltage	$I_F = 10\text{ mA}$; see Fig.4	0.9	V
I_R	reverse current			
	BZV55-B/F/C2V4	$V_R = 1\text{ V}$	50	μA
	BZV55-B/F/C2V7	$V_R = 1\text{ V}$	20	μA
	BZV55-B/F/C3V0	$V_R = 1\text{ V}$	10	μA
	BZV55-B/F/C3V3	$V_R = 1\text{ V}$	5	μA
	BZV55-B/F/C3V6	$V_R = 1\text{ V}$	5	μA
	BZV55-B/F/C3V9	$V_R = 1\text{ V}$	3	μA
	BZV55-B/F/C4V3	$V_R = 1\text{ V}$	3	μA
	BZV55-B/F/C4V7	$V_R = 2\text{ V}$	3	μA
	BZV55-B/F/C5V1	$V_R = 2\text{ V}$	2	μA
	BZV55-B/F/C5V6	$V_R = 2\text{ V}$	1	μA
	BZV55-B/F/C6V2	$V_R = 4\text{ V}$	3	μA
	BZV55-B/F/C6V8	$V_R = 4\text{ V}$	2	μA
	BZV55-B/F/C7V5	$V_R = 5\text{ V}$	1	μA
	BZV55-B/F/C8V2	$V_R = 5\text{ V}$	700	nA
	BZV55-B/F/C9V1	$V_R = 6\text{ V}$	500	nA
	BZV55-B/F/C10	$V_R = 7\text{ V}$	200	nA
	BZV55-B/F/C11	$V_R = 8\text{ V}$	100	nA
	BZV55-B/F/C12	$V_R = 8\text{ V}$	100	nA
	BZV55-B/F/C13	$V_R = 8\text{ V}$	100	nA
	BZV55-B/F/C15 to 75	$V_R = 0.7V_{Znom}$	50	nA

Voltage regulator diodes

BZV55 series

Table 1 Per type BZV55-B/F/C2V4 to B/F/C24
 $T_J = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

BZV55-B or F or C XXX	WORKING VOLTAGE V _Z (V) at I _{Ztest} = 5 mA						DIFFERENTIAL RESISTANCE r _{diff} (Ω)						TEMP. COEFF. S _Z (mV/K) at I _{Ztest} = 5 mA (see Figs 5 and 6)			DIODE CAP. C _d (pF) at f = 1 MHz; V _R = 0 V	NON-REPETITIVE PEAK REVERSE CURRENT I _{ZSM} (A) at t _p = 100 μs; T _{amb} = 25 °C
	Tol. ±2% (B)		Tol. ±3% (F)		Tol. ±5% (C)		at I _{Ztest} = 1 mA			at I _{Ztest} = 5 mA							
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	TYP.	MAX.	TYP.	MAX.	MIN.	TYP.	MAX.				
2V4	2.35	2.45	2.33	2.47	2.2	2.6	275	600	70	100	-3.5	-1.6	0	450	6.0		
2V7	2.65	2.75	2.62	2.78	2.5	2.9	300	600	75	100	-3.5	-2.0	0	450	6.0		
3V0	2.94	3.06	2.91	3.09	2.8	3.2	325	600	80	95	-3.5	-2.1	0	450	6.0		
3V3	3.23	3.37	3.20	3.40	3.1	3.5	350	600	85	95	-3.5	-2.4	0	450	6.0		
3V6	3.53	3.67	3.49	3.71	3.4	3.8	375	600	85	90	-3.5	-2.4	0	450	6.0		
3V9	3.82	3.98	3.78	4.02	3.7	4.1	400	600	85	90	-3.5	-2.5	0	450	6.0		
4V3	4.21	4.39	4.17	4.43	4.0	4.6	410	600	80	90	-3.5	-2.5	0	450	6.0		
4V7	4.61	4.79	4.56	4.84	4.4	5.0	425	500	50	80	-3.5	-1.4	0.2	300	6.0		
5V1	5.00	5.20	4.95	5.25	4.8	5.4	400	480	40	60	-2.7	-0.8	1.2	300	6.0		
5V6	5.49	5.71	5.43	5.77	5.2	6.0	80	400	15	40	-2.0	1.2	2.5	300	6.0		
6V2	6.08	6.32	6.01	6.39	5.8	6.6	40	150	6	10	0.4	2.3	3.7	200	6.0		
6V8	6.66	6.94	6.60	7.00	6.4	7.2	30	80	6	15	1.2	3.0	4.5	200	6.0		
7V5	7.35	7.65	7.28	7.72	7.0	7.9	30	80	6	15	2.5	4.0	5.3	150	4.0		
8V2	8.04	8.36	7.95	8.45	7.7	8.7	40	80	6	15	3.2	4.6	6.2	150	4.0		
9V1	8.92	9.28	8.83	9.37	8.5	9.6	40	100	6	15	3.8	5.5	7.0	150	3.0		
10	9.80	10.20	9.70	10.30	9.4	10.6	50	150	8	20	4.5	6.4	8.0	90	3.0		
11	10.80	11.20	10.67	11.33	10.4	11.6	50	150	10	20	5.4	7.4	9.0	85	2.5		
12	11.80	12.20	11.64	12.36	11.4	12.7	50	150	10	25	6.0	8.4	10.0	85	2.5		
13	12.70	13.30	12.61	13.39	12.4	14.1	50	170	10	30	7.0	9.4	11.0	80	2.5		
15	14.70	15.30	14.55	15.45	13.8	15.6	50	200	10	30	9.2	11.4	13.0	75	2.0		
16	15.70	16.30	15.50	16.50	15.3	17.1	50	200	10	40	10.4	12.4	14.0	75	1.5		
18	17.60	18.40	17.50	18.50	16.8	19.1	50	225	10	45	12.4	14.4	16.0	70	1.5		
20	19.60	20.40	19.40	20.60	18.8	21.2	60	225	15	55	14.4	16.4	18.0	60	1.5		
22	21.60	22.40	21.30	22.70	20.8	23.3	60	250	20	55	16.4	18.4	20.0	60	1.25		
24	23.50	24.50	23.30	24.70	22.8	25.6	60	250	25	70	18.4	20.4	22.0	55	1.25		

Voltage regulator diodes

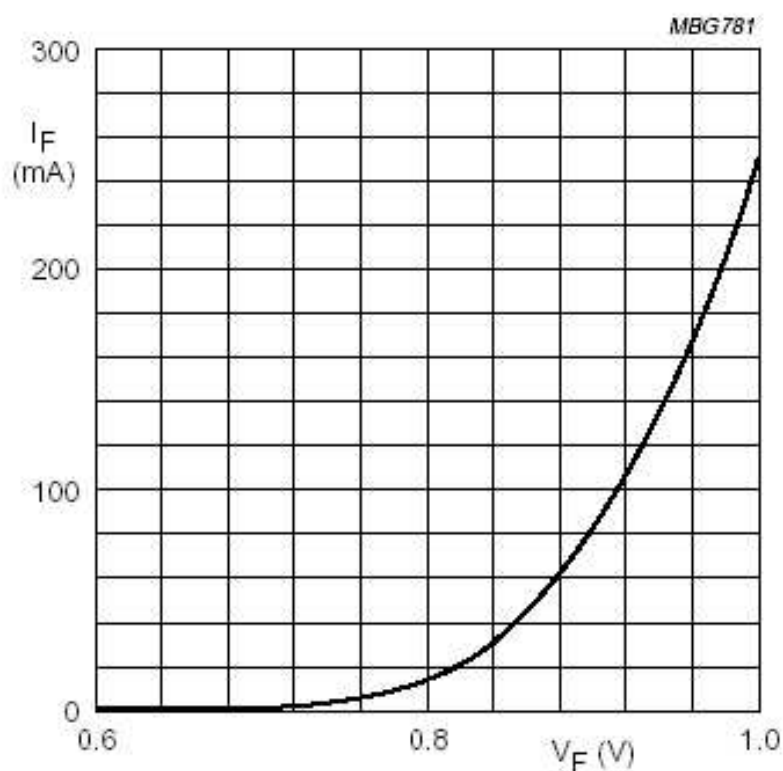
BZV55 series

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-tp}$	thermal resistance from junction to tie-point		300	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient	see Fig.2 and note 1	380	K/W

Note

1. Device mounted on a ceramic substrate of $10 \times 10 \times 0.6$ mm.



$T_j = 25^\circ\text{C}$.

Fig.4 Forward current as a function of forward voltage; typical values.



ICL7660S

April 1994

Super Voltage Converter

Features

- Guaranteed Lower Max Supply Current for All Temperature Ranges
- Wide Operating Voltage Range 1.5V to 12V
- 100% Tested at 3V
- No External Diode Over Full Temperature and Voltage Range
- Boost Pin (Pin 1) for Higher Switching Frequency
- Guaranteed Minimum Power Efficiency of 96%
- Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%
- Improved SCR Latchup Protection
- Simple Conversion of +5V Logic Supply to $\pm 5V$ Supplies
- Simple Voltage Multiplication $V_{OUT} = (-)nV_{IN}$
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- Improved Direct Replacement for Industry Standard ICL7660 and Other Second Source Devices

Applications

- Simple Conversion of +5V to $\pm 5V$ Supplies
- Voltage Multiplication $V_{OUT} = \pm nV_{IN}$
- Negative Supplies for Data Acquisition Systems and Instrumentation
- RS232 Power Supplies
- Supply Splitter, $V_{OUT} = \pm V_S/2$

Description

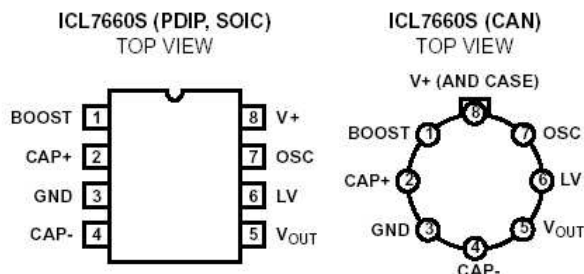
The ICL7660S Super Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry standard ICL7660 offering an **extended** operating supply voltage range up to 12V, with **lower** supply current. **No external diode** is needed for the ICL7660S. In addition, a **Frequency Boost pin** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in the Electrical Specifications section. **Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.**

The ICL7660S performs supply voltage conversion from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of -1.5V to -12V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660S can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

Pinouts



Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
ICL7660SCBA	0°C to +70°C	8 Lead Plastic SOIC (N)
ICL7660SCPA	0°C to +70°C	8 Lead Plastic DIP
ICL7660SCTV	0°C to +70°C	8 Pin Metal Can
ICL7660SIBA	-40°C to +85°C	8 Lead Plastic SOIC (N)
ICL7660SIPA	-40°C to +85°C	8 Lead Plastic DIP
ICL7660SITV	-40°C to +85°C	8 Pin Metal Can
ICL7660SMTV (Note)	-55°C to +125°C	8 Pin Metal Can

NOTE: Add /883B to part number if 883B processing is required.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3179.1**

7-118

Specifications ICL7660S**Absolute Maximum Ratings**

Supply Voltage	+13.0V
LV and OSC Input Voltage (Note 1)	
V+ < 5.5V	-0.3V to V+ + 0.3V
V+ > 5.5V	V+ -5.5V to V+ +0.3V
Current into LV (Note 1)	
V+ > 3.5V	20 μ A
Output Short Duration	
V _{SUPPLY} $\leq$ 5.5V	Continuous
Storage Temperature Range	-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP	150°C/W	-
Plastic SOIC	170°C/W	-
Metal Can	155°C/W	70°C/W
Lead Temperature (Soldering 10s)		+300°C
(SOIC - Lead Tips Only)		

Operating Conditions

Operating Temperature Range	ICL7660SI	-40°C to +85°C
ICL7660SM		-55°C to +125°C
	ICL7660SC	0°C to +70°C

Electrical Specifications V+ = 5V, T_A = +25°C, OSC = Free running, Test Circuit Figure 12, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 3)	I+	R _L = ∞ , +25°C	-	80	160	μ A
		0°C < T _A < +70°C	-	-	180	μ A
		-40°C < T _A < +85°C	-	-	180	μ A
		-55°C < T _A < +125°C	-	-	200	μ A
Supply Voltage Range - High (Note 4)	V _H	R _L = 10K, LV Open, T _{MIN} < T _A < T _{MAX}	3.0	-	12	V
Supply Voltage Range - Low	V _L	R _L = 10K, LV to GND, T _{MIN} < T _A < T _{MAX}	1.5	-	3.5	V
Output Source Resistance	R _{OUT}	I _{OUT} = 20mA	-	60	100	Ω
		I _{OUT} = 20mA, 0°C < T _A < +70°C	-	-	120	Ω
		I _{OUT} = 20mA, -25°C < T _A < +85°C	-	-	120	Ω
		I _{OUT} = 20mA, -55°C < T _A < +125°C	-	-	150	Ω
		I _{OUT} = 3mA, V+ = 2V, LV = GND, 0°C < T _A < +70°C	-	-	250	Ω
		I _{OUT} = 3mA, V+ = 2V, LV = GND, -40°C < T _A < +85°C	-	-	300	Ω
		I _{OUT} = 3mA, V+ = 2V, LV = GND, -55°C < T _A < +125°C	-	-	400	Ω
Oscillator Frequency (Note 3)	f _{OSC}	C _{OSC} = 0, Pin 1 Open or GND	5	10	-	kHz
		C _{OSC} = 0, Pin 1 = V+	-	35	-	kHz
Power Efficiency	P _{EFF}	R _L = 5k Ω	96	98	-	%
		T _{MIN} < T _A < T _{MAX} R _L = 5k Ω	95	97	-	-
Voltage Conversion Efficiency	V _{OUT} EFF	R _L = ∞	99	99.9	-	%
Oscillator Impedance	Z _{OSC}	V+ = 2V	-	1	-	M Ω
		V+ = 5V	-	100	-	k Ω

NOTES:

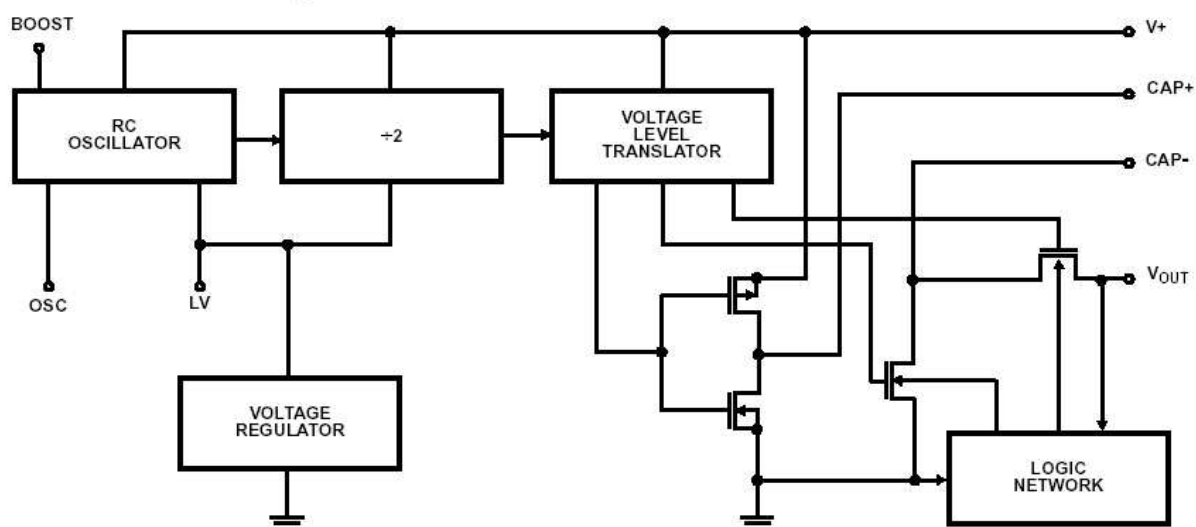
- Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660S.
- Derate linearly above +50°C by 5.5mW/°C
- In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
- The Harris ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.
- All significant improvements over the industry standard ICL7660 are highlighted.

Specifications ICL7660S**Electrical Specifications**V+ = 3V, T_A = +25°C, OSC = Free running, Test Circuit Figure 12, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 3)	I ₊	V+ = 3V, R _L = ∞, +25°C	-	26	100	μA
		0°C < T _A < +70°C	-	-	125	μA
		-40°C < T _A < +85°C	-	-	125	μA
		-55°C < T _A < +125°C	-	-	150	μA
Output Source Resistance	R _{OUT}	V+ = 3V, I _{OUT} = 10mA	-	97	150	Ω
		0°C < T _A < +70°C	-	-	200	Ω
		-40°C < T _A < +85°C	-	-	200	Ω
		-55°C < T _A < +125°C	-	-	250	Ω
Oscillator Frequency (Note 3)	f _{OSC}	V+ = 3V (same as 5V conditions)	2.5	4	-	kHz
		0°C < T _A < +70°C	1.5	-	-	kHz
		-40°C < T _A < +85°C	1.5	-	-	kHz
		-55°C < T _A < +125°C	1.0	-	-	kHz
Voltage Conversion Efficiency	V _{OUT} EFF	V+ = 3V, R _L = ∞	99	-	-	%
		T _{MIN} < T _A < T _{MAX}	99	-	-	%
Power Efficiency	P _{EFF}	V+ = 3V, R _L = 5kΩ	96	-	-	%
		T _{MIN} < T _A < T _{MAX}	95	-	-	%

NOTES:

1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660S.
2. Derate linearly above +50°C by 5.5mW/°C
3. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
4. The Harris ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.
5. All significant improvements over the industry standard ICL7660 are highlighted.

Functional Block Diagram

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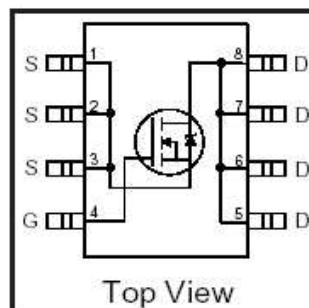
HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- N-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

Description

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



$$V_{DS} = 30V$$

$$R_{DS(on)} = 0.030\Omega$$



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	30	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	7.3	A
$I_D @ T_C = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.8	
I_{DM}	Pulsed Drain Current ①	58	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.5	W
$P_D @ T_C = 70^\circ C$	Power Dissipation	1.6	
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
V_{GSM}	Gate-to-Source Voltage Single Pulse $t_p < 10\mu s$	30	V
E_{AS}	Single Pulse Avalanche Energy ②	70	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	50	°C/W

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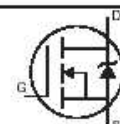
International
IR RectifierElectrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.024	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.030	Ω	$V_{GS} = 10V, I_D = 7.3A$ ④
		—	—	0.050		$V_{GS} = 4.5V, I_D = 3.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	5.8	—	—	S	$V_{DS} = 15V, I_D = 2.3A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	19	28	nC	$I_D = 4.6A$
Q_{gs}	Gate-to-Source Charge	—	2.3	3.5		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	6.3	9.5		$V_{GS} = 10V$, See Fig. 10 ④
$t_{d(on)}$	Turn-On Delay Time	—	7.0	—	ns	$V_{DD} = 15V$
t_r	Rise Time	—	35	—		$I_D = 4.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	19	—		$R_D = 3.2\Omega$, ⑤
C_{iss}	Input Capacitance	—	550	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	260	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—		$f = 1.0\text{MHz}$, See Fig. 9

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	58		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 4.6A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	48	73	ns	$T_J = 25^\circ\text{C}, I_F = 4.6A$
Q_{rr}	Reverse Recovery Charge	—	73	110	nC	$di/dt = 100A/\mu s$ ③

Notes:

① Repetitive rating; pulse width limited by
max. junction temperature. (See fig. 11)② $V_{DD} = 15V$, starting $T_J = 25^\circ\text{C}$, $L = 6.6\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 4.6A$. (See Figure 8)③ $I_{SD} \leq 4.6A$, $di/dt \leq 120A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$ ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.⑤ When mounted on 1 inch square copper board, $t < 10$ sec

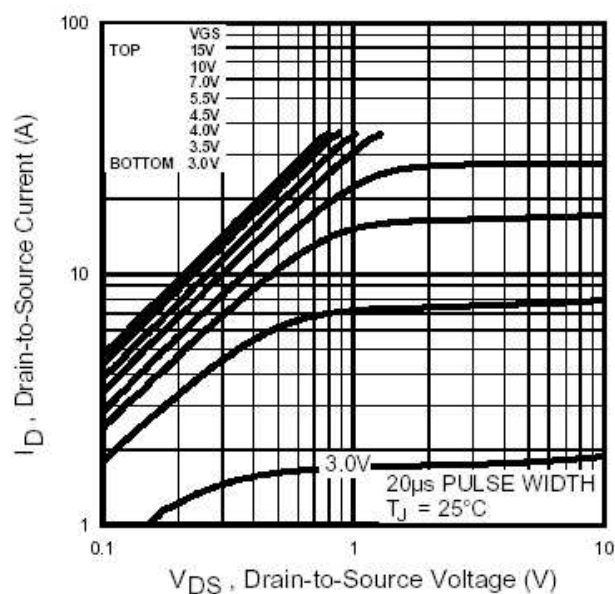


Fig 1. Typical Output Characteristics

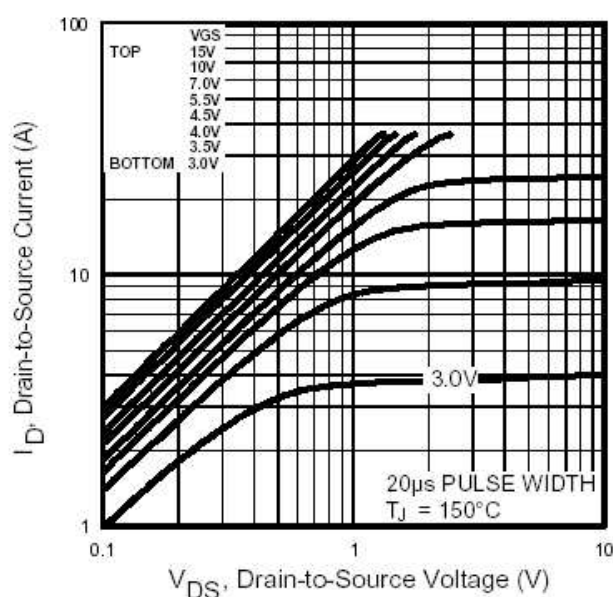


Fig 2. Typical Output Characteristics

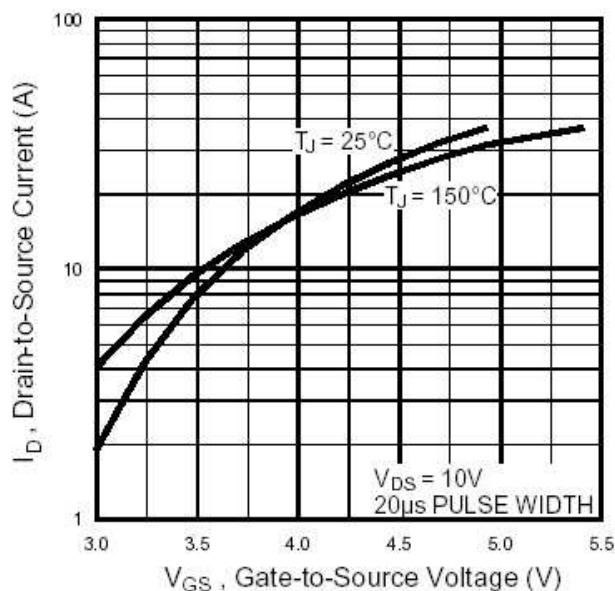


Fig 3. Typical Transfer Characteristics

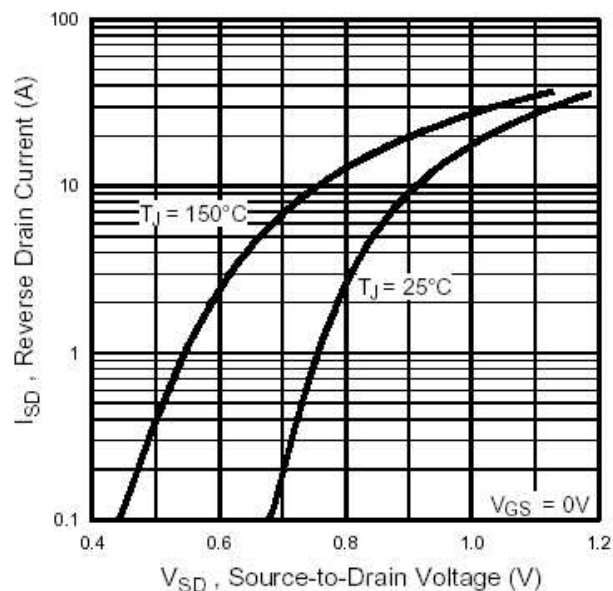


Fig 4. Typical Source-Drain Diode Forward Voltage

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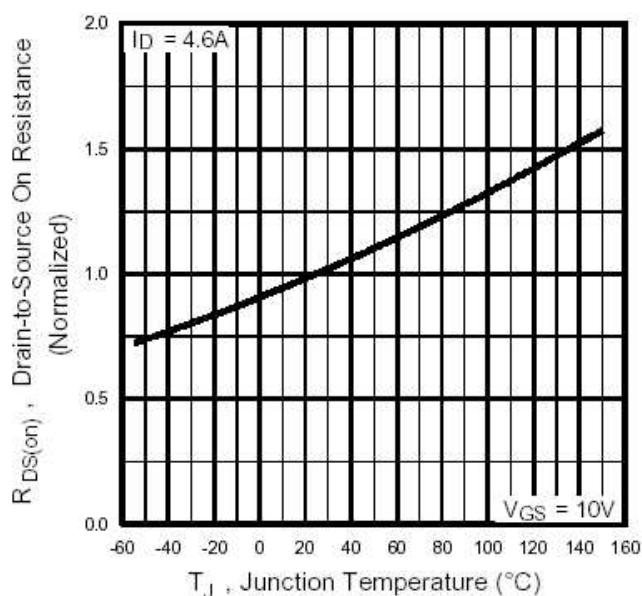
International
IR Rectifier

Fig 5. Normalized On-Resistance
Vs. Temperature

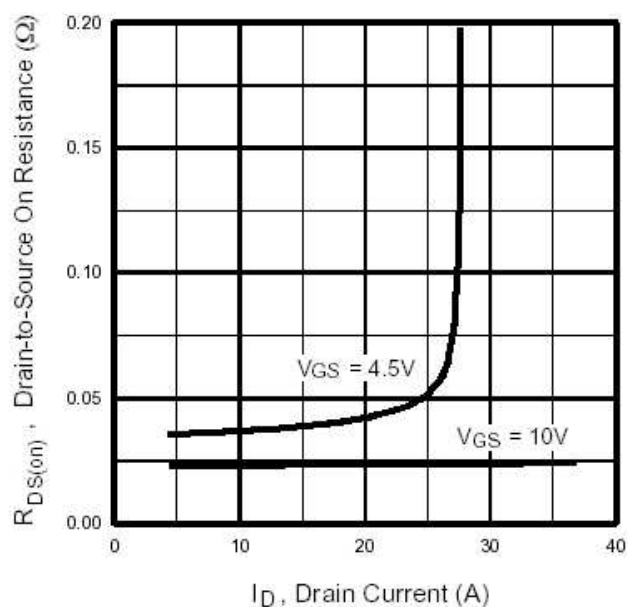


Fig 6. On-Resistance Vs. Drain Current

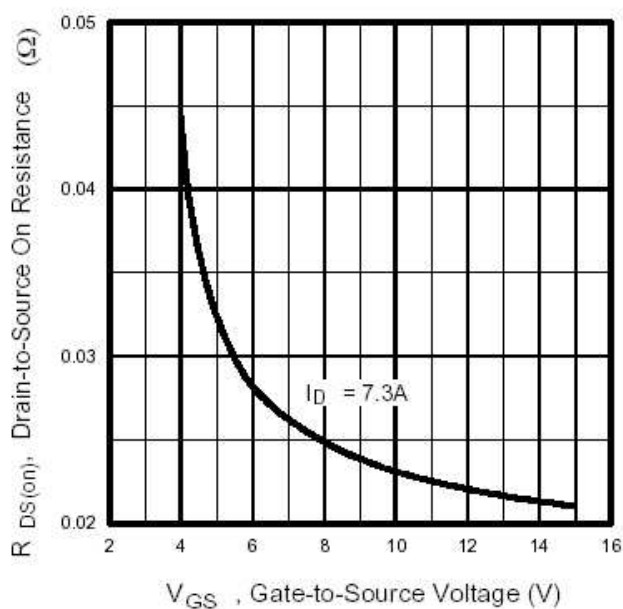


Fig 7. On-Resistance Vs. Gate Voltage

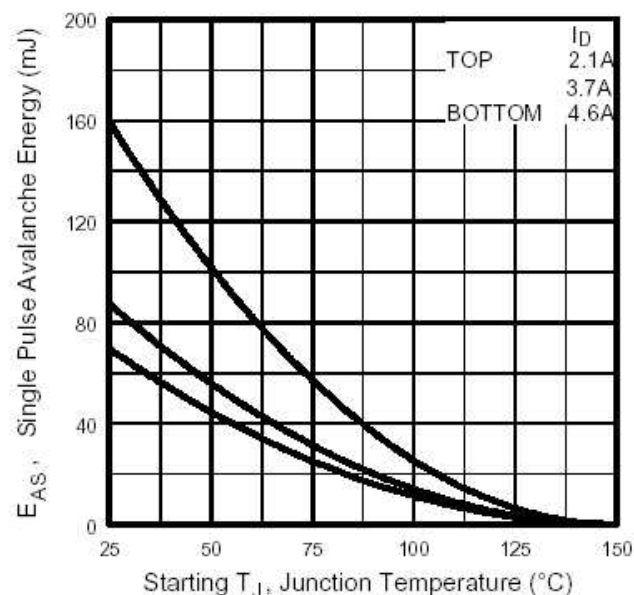


Fig 8. Maximum Avalanche Energy
Vs. Drain Current

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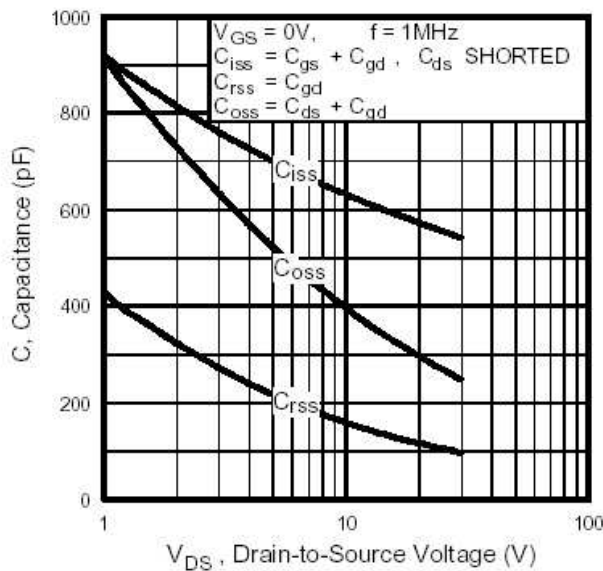


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

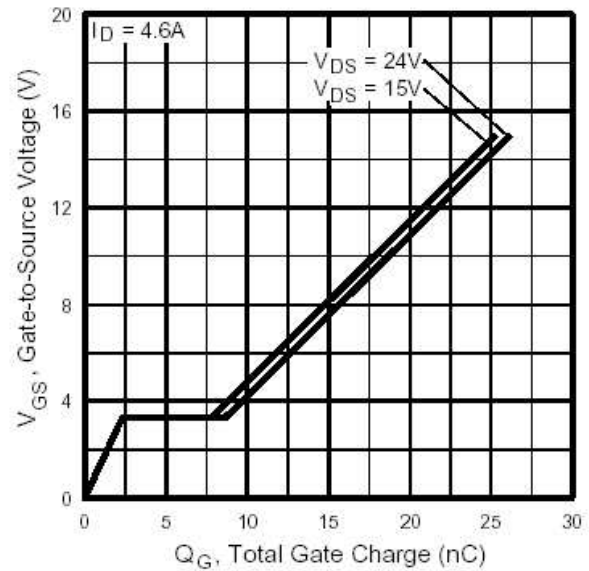


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

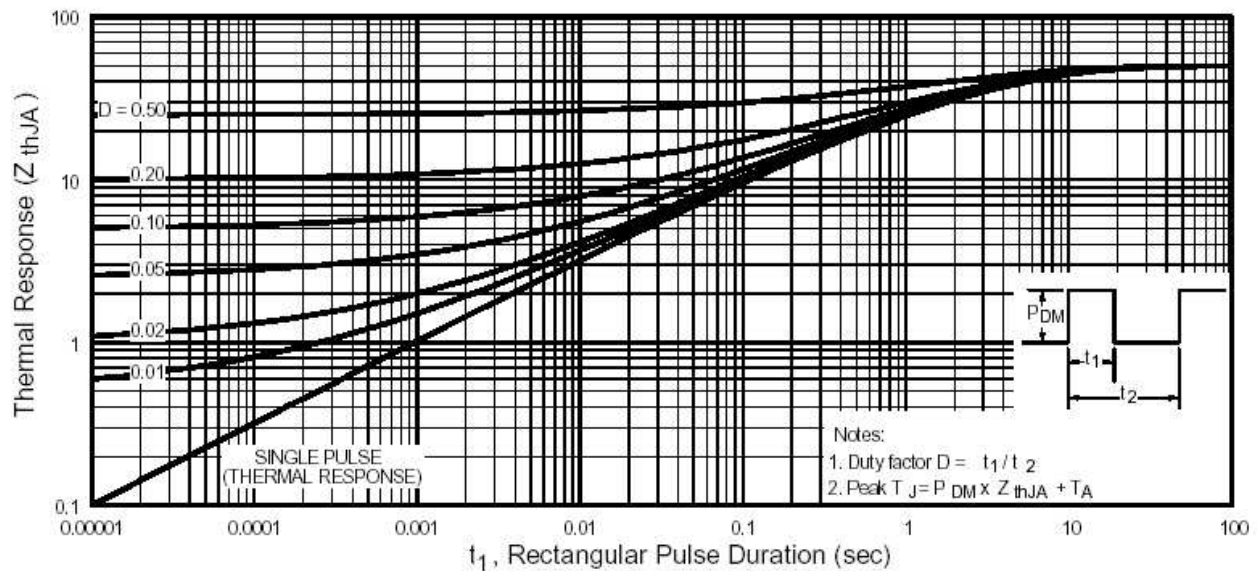


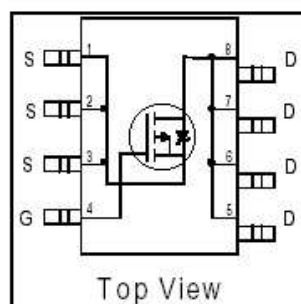
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

- Advanced Process Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

Description

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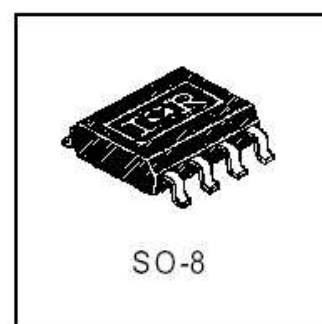


Top View

$$V_{DS} = -30V$$

$$R_{DS(on)} = 0.070\Omega$$

$$I_D = -4.6A$$



SO-8

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-4.6	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-3.7	
I_{DM}	Pulsed Drain Current ①	-15	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.5	W
	Linear Derating Factor	0.020	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	-3.0	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C

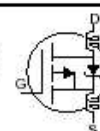
Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	50	°C/W

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International
IOR RectifierElectrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.024	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.070	Ω	$V_{GS} = -10V$, $I_D = -4.6A$ ③
		—	—	0.130		$V_{GS} = -4.5V$, $I_D = -2.0A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-3.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	—	6.6	—	S	$V_{DS} = -15V$, $I_D = -4.6A$ ③
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -24V$, $V_{GS} = 0V$
		—	—	-5.0		$V_{DS} = -15V$, $V_{GS} = 0V$, $T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	27	40	nC	$I_D = -4.6A$
Q_{gs}	Gate-to-Source Charge	—	5.2	—		$V_{DS} = -15V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	7.5	—		$V_{GS} = -10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	14	30	ns	$V_{DD} = -15V$
t_r	Rise Time	—	21	60		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	97	150		$R_G = 6.0\Omega$
t_f	Fall Time	—	71	100		$R_D = 10\Omega$ ③
L_D	Internal Drain Inductance	—	2.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	4.0	—		
C_{iss}	Input Capacitance	—	870	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	720	—		$V_{DS} = -10V$
C_{rss}	Reverse Transfer Capacitance	—	220	—		$f = 1.0MHz$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-15		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}$, $I_S = -1.25A$, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	70	100	ns	$T_J = 25^\circ\text{C}$, $I_F = -4.6A$
Q_{rr}	Reverse Recovery Charge	—	100	180	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② $I_{SD} \leq -4.6A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10sec$.

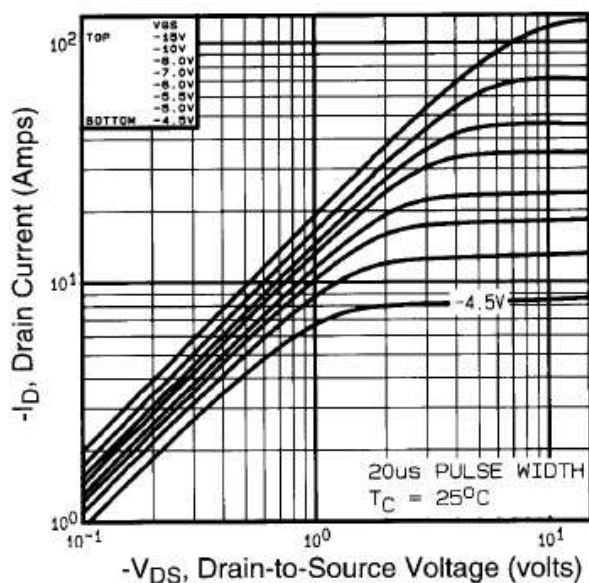


Fig 1. Typical Output Characteristics,

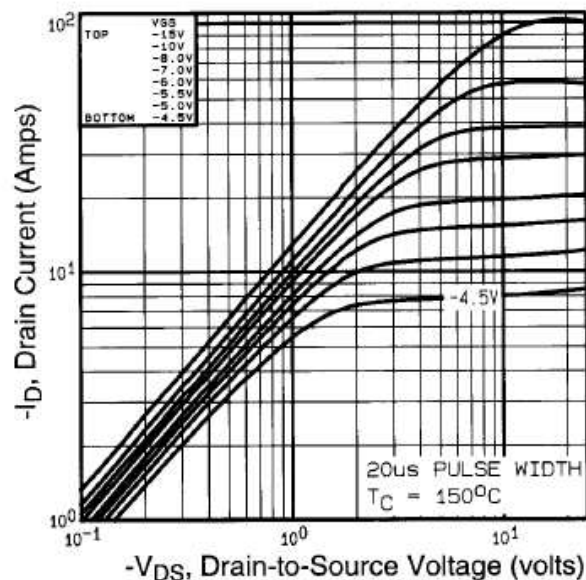


Fig 2. Typical Output Characteristics,

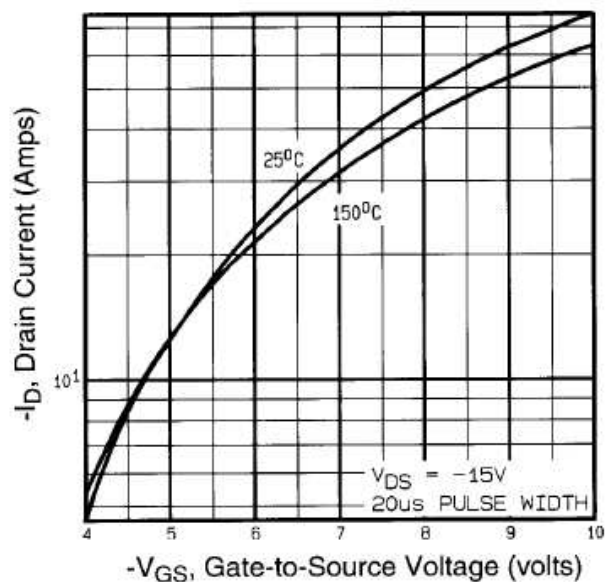


Fig 3. Typical Transfer Characteristics

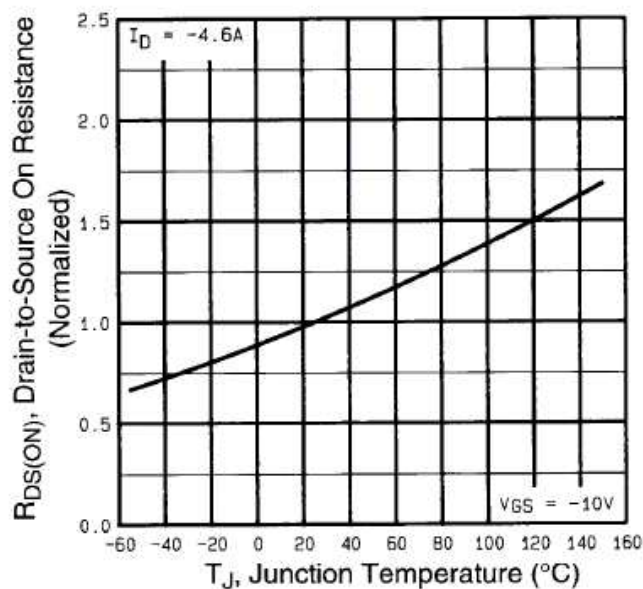


Fig 4. Normalized On-Resistance Vs. Temperature

IRF7205

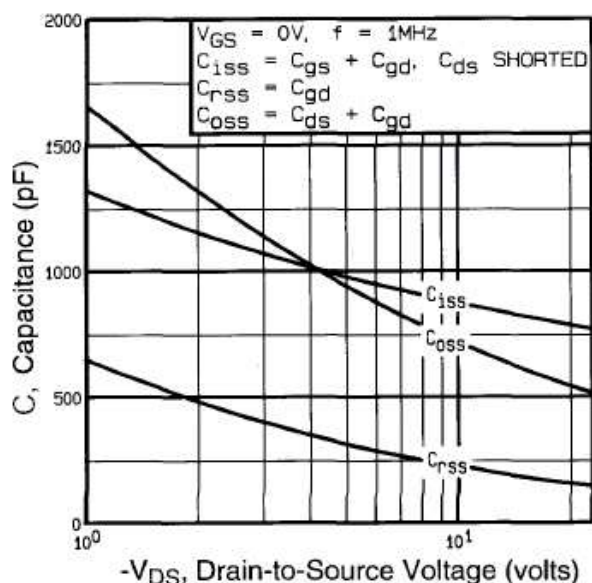
International
IOR Rectifier

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

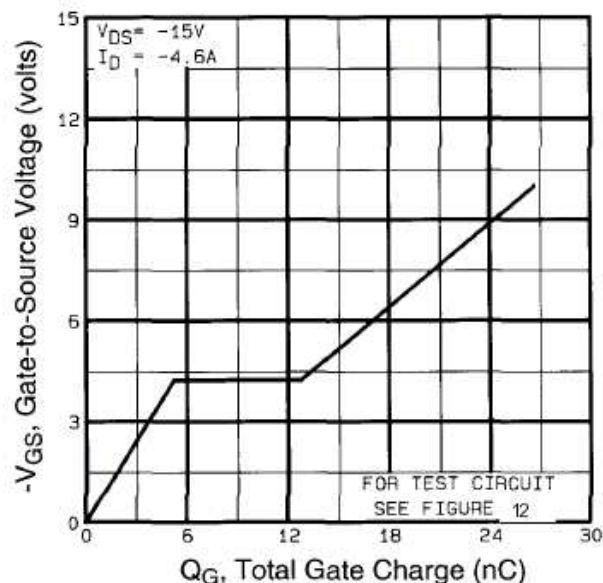


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

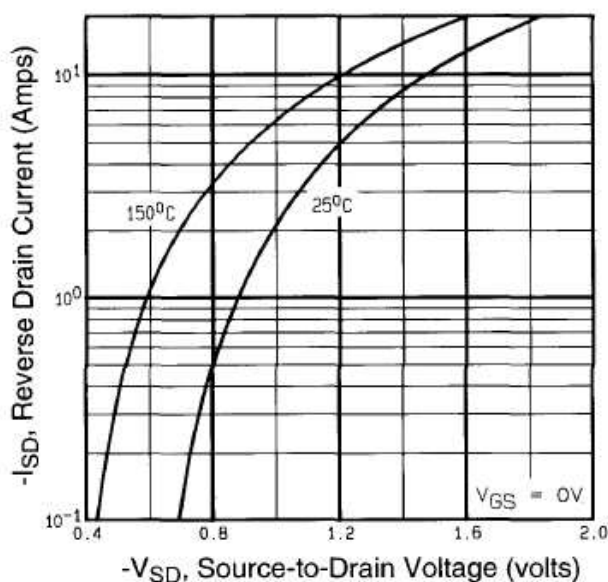


Fig 7. Typical Source-Drain Diode Forward Voltage

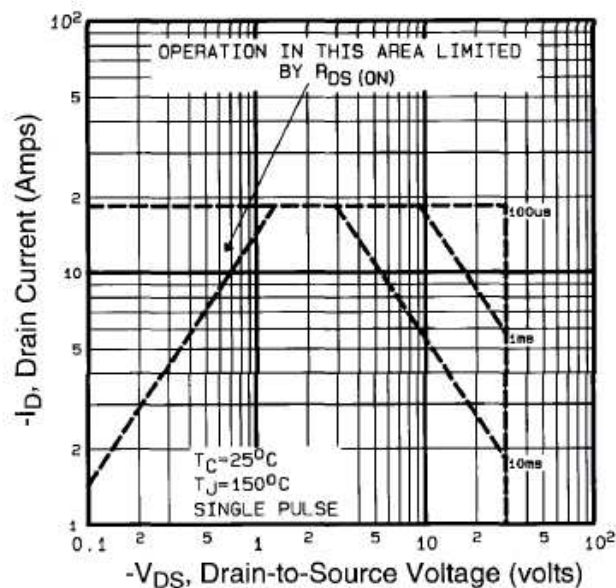


Fig 8. Maximum Safe Operating Area

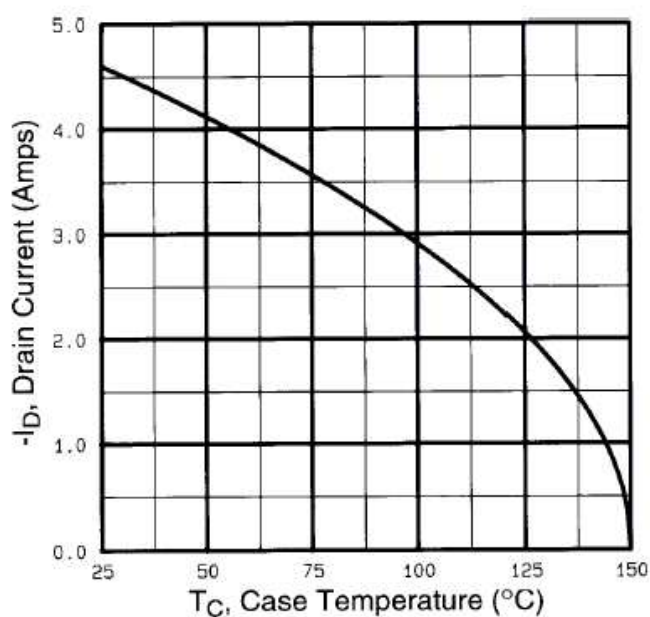


Fig 9. Maximum Drain Current Vs. Case Temperature

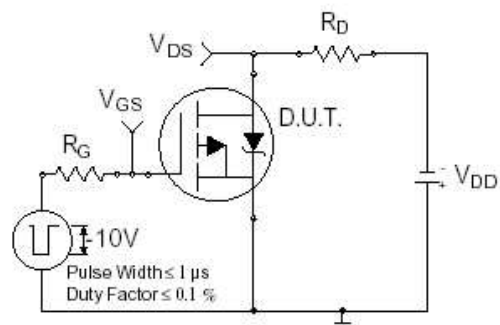


Fig 10a. Switching Time Test Circuit

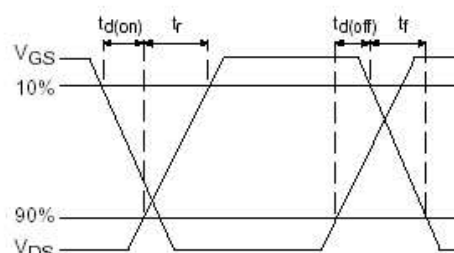


Fig 10b. Switching Time Waveforms

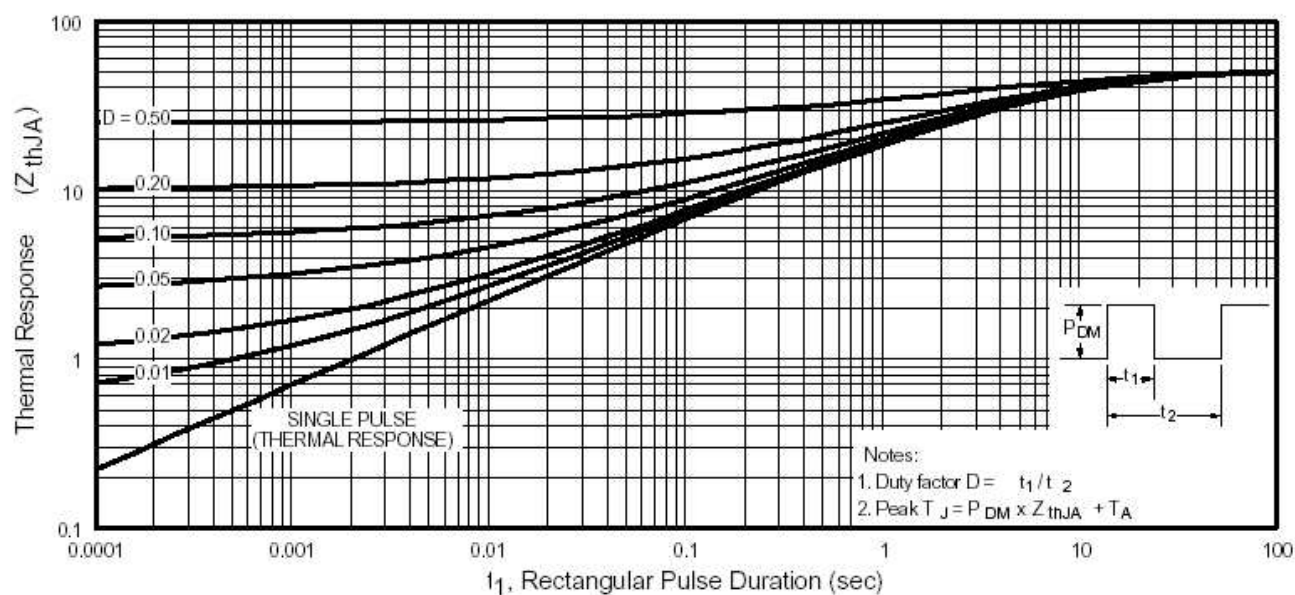


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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MC78L00, A Series

MAXIMUM RATINGS ($T_A = +125^\circ\text{C}$, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	0 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_I = 10\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC78LXXAB), $0^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L05AC, AB			MC78L05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) 7.0 Vdc $\leq V_I \leq 20\text{ Vdc}$ 8.0 Vdc $\leq V_I \leq 20\text{ Vdc}$	Reg_{line}	– –	55 45	150 100	– –	55 45	200 150	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Reg_{load}	– –	11 5.0	60 30	– –	11 5.0	60 30	mV
Output Voltage (7.0 Vdc $\leq V_I \leq 20\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 10\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	4.75 4.75	– –	5.25 5.25	4.5 4.5	– –	5.5 5.5	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	– –	3.8 –	6.0 5.5	– –	3.8 –	6.0 5.5	mA
Input Bias Current Change (8.0 Vdc $\leq V_I \leq 20\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	– –	– –	1.5 0.1	– –	– –	1.5 0.2	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	–	40	–	–	40	–	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $8.0\text{ Vdc} \leq V_I \leq 18\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	41	49	–	40	49	–	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS ($V_I = 14\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC78LXXAB), $0^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L08AC, AB			MC78L08C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) 10.5 Vdc $\leq V_I \leq 23\text{ Vdc}$ 11 Vdc $\leq V_I \leq 23\text{ Vdc}$	Reg_{line}	– –	20 12	175 125	– –	20 12	200 150	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Reg_{load}	– –	15 8.0	80 40	– –	15 6.0	80 40	mV
Output Voltage (10.5 Vdc $\leq V_I \leq 23\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 14\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	7.6 7.6	– –	8.4 8.4	7.2 7.2	– –	8.8 8.8	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	– –	3.0 –	6.0 5.5	– –	3.0 –	6.0 5.5	mA
Input Bias Current Change (11 Vdc $\leq V_I \leq 23\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	– –	– –	1.5 0.1	– –	– –	1.5 0.2	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	–	60	–	–	52	–	μV
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $12\text{ V} \leq V_I \leq 23\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	37	57	–	35	55	–	dB
Dropout Voltage ($T_J = +25^\circ\text{C}$)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

MC78L00, A Series

Figure 1. Dropout Characteristics

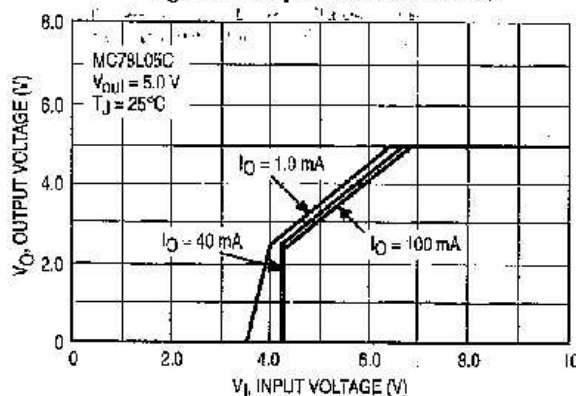


Figure 2. Dropout Voltage versus Junction Temperature

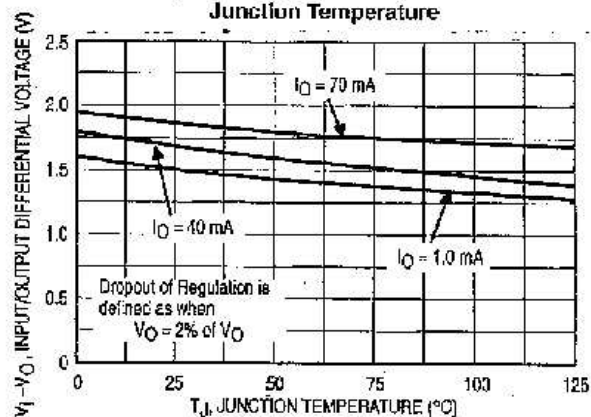


Figure 3. Input Bias Current versus Ambient Temperature

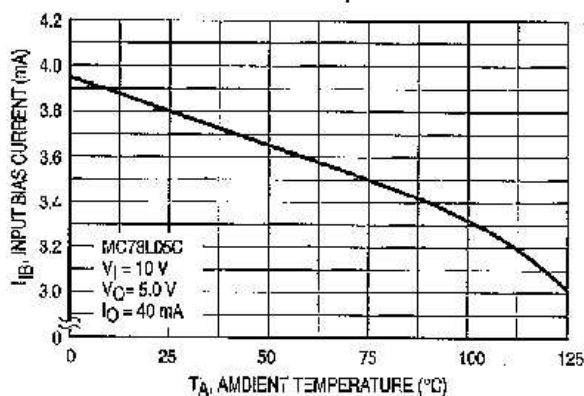


Figure 4. Input Bias Current versus Input Voltage

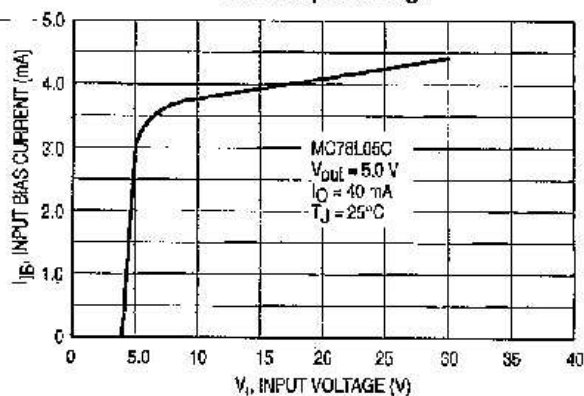
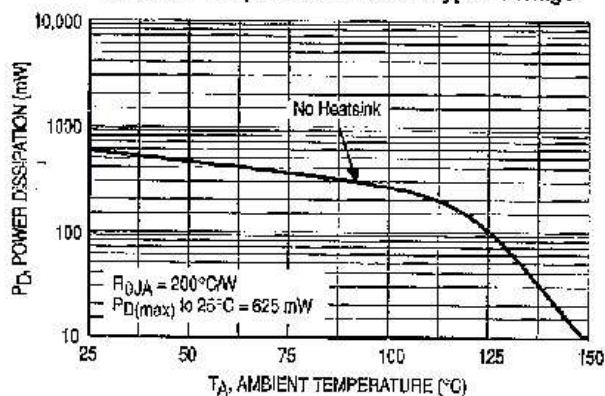


Figure 5. Maximum Average Power Dissipation versus Ambient Temperature – TO-92 Type Package



P6KE6.8A Series

600 Watt Peak Power Surmetic™ -40 Zener Transient Voltage Suppressors

Unidirectional*

The P6KE6.8A series is designed to protect voltage sensitive components from high voltage, high energy transients. They have excellent clamping capability, high surge capability, low zener impedance and fast response time. These devices are ON Semiconductor's exclusive, cost-effective, highly reliable Surmetic™ axial leaded package and is ideally-suited for use in communication systems, numerical controls, process controls, medical equipment, business machines, power supplies and many other industrial/consumer applications.

Specification Features:

- Working Peak Reverse Voltage Range – 5.8 to 171 V
- Peak Power – 600 Watts @ 1 ms
- ESD Rating of Class 3 (>16 KV) per Human Body Model
- Maximum Clamp Voltage @ Peak Pulse Current
- Low Leakage < 5 μ A above 10 V
- Maximum Temperature Coefficient Specified
- UL 497B for Isolated Loop Circuit Protection
- Response Time is typically < 1 ns

Mechanical Characteristics:

CASE: Void-free, Transfer-molded, Thermosetting plastic

FINISH: All external surfaces are corrosion resistant and leads are readily solderable

MAXIMUM LEAD TEMPERATURE FOR SOLDERING:

230°C, 1/16" from the case for 10 seconds

POLARITY: Cathode indicated by polarity band

MOUNTING POSITION: Any

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation (Note 1.) @ $T_L \leq 25^\circ\text{C}$	P_{PK}	600	Watts
Steady State Power Dissipation @ $T_L \leq 75^\circ\text{C}$, Lead Length = 3/8" Derated above $T_L = 75^\circ\text{C}$	P_D	5.0 50	Watts mW/°C
Thermal Resistance, Junction-to-Lead	$R_{\theta JL}$	15	°C/W
Forward Surge Current (Note 2.) @ $T_A = 25^\circ\text{C}$	I_{FSM}	100	Amps
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C

1. Nonrepetitive current pulse per Figure 4 and derated above $T_A = 25^\circ\text{C}$ per Figure 2.

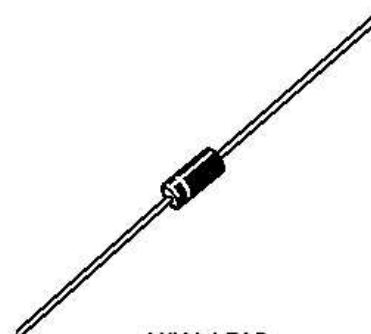
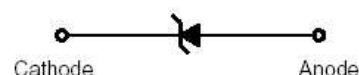
2. 1/2 sine wave (or equivalent square wave), $PW = 8.3$ ms, duty cycle = 4 pulses per minute maximum.

*Please see P6KE6.8CA – P6KE200CA for Bidirectional devices.



ON Semiconductor™

<http://onsemi.com>



AXIAL LEAD
CASE 17
STYLE 1



L = Assembly Location
P6KExxxA = ON Device Code
YY = Year
WW = Work Week

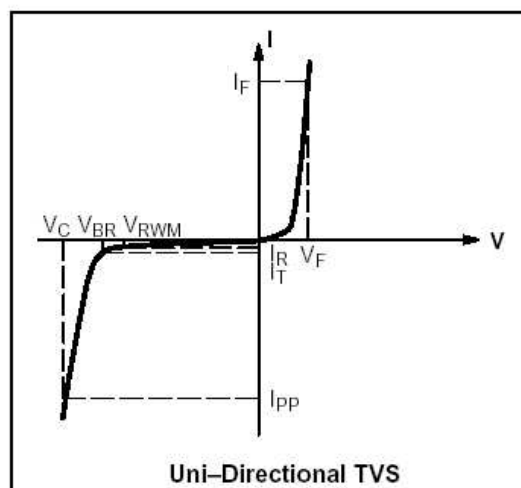
ORDERING INFORMATION

Device	Package	Shipping
P6KExxxA	Axial Lead	1000 Units/Box
P6KExxxARL	Axial Lead	4000/Tape & Reel

P6KE6.8A Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 3.5\text{ V Max. @ } I_F \text{ (Note 6.)} = 50\text{ A}$)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
ΘV_{BR}	Maximum Temperature Coefficient of V_{BR}
I_F	Forward Current
V_F	Forward Voltage @ I_F



P6KE6.8A Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 3.5\text{ V Max. @ } I_F \text{ (Note 6.)} = 50\text{ A}$)

Device	Device Marking	V_{RWM} (Note 3.)	$I_R @ V_{RWM}$	Breakdown Voltage				$V_C @ I_{PP}$ (Note 5.)		θV_{BR}
				V_{BR} (Note 4.) (Volts)			@ I_T	V_C	I_{PP}	
		Volts	μA	Min	Nom	Max	mA	Volts	A	$^\circ\text{C}$
P6KE6.8A	P6KE6.8A	5.8	1000	6.45	6.80	7.14	10	10.5	57	0.057
P6KE7.5A	P6KE7.5A	6.4	500	7.13	7.51	7.88	10	11.3	53	0.061
P6KE8.2A	P6KE8.2A	7.02	200	7.79	8.2	8.61	10	12.1	50	0.065
P6KE9.1A	P6KE9.1A	7.78	50	8.65	9.1	9.55	1	13.4	45	0.068
P6KE10A	P6KE10A	8.55	10	9.5	10	10.5	1	14.5	41	0.073
P6KE11A	P6KE11A	9.4	5	10.5	11.05	11.6	1	15.6	38	0.075
P6KE12A	P6KE12A	10.2	5	11.4	12	12.6	1	16.7	36	0.078
P6KE13A	P6KE13A	11.1	5	12.4	13.05	13.7	1	18.2	33	0.081
P6KE15A	P6KE15A	12.8	5	14.3	15.05	15.8	1	21.2	28	0.084
P6KE16A	P6KE16A	13.6	5	15.2	16	16.8	1	22.5	27	0.086
P6KE18A	P6KE18A	15.3	5	17.1	18	18.9	1	25.2	24	0.088
P6KE20A	P6KE20A	17.1	5	19	20	21	1	27.7	22	0.09
P6KE22A	P6KE22A	18.8	5	20.9	22	23.1	1	30.6	20	0.092
P6KE24A	P6KE24A	20.5	5	22.8	24	25.2	1	33.2	18	0.094
P6KE27A	P6KE27A	23.1	5	25.7	27.05	28.4	1	37.5	16	0.096
P6KE30A	P6KE30A	25.6	5	28.5	30	31.5	1	41.4	14.4	0.097
P6KE33A	P6KE33A	28.2	5	31.4	33.05	34.7	1	45.7	13.2	0.098
P6KE36A	P6KE36A	30.8	5	34.2	36	37.8	1	49.9	12	0.099
P6KE39A	P6KE39A	33.3	5	37.1	39.05	41	1	53.9	11.2	0.1
P6KE43A	P6KE43A	36.8	5	40.9	43.05	45.2	1	59.3	10.1	0.101
P6KE47A	P6KE47A	40.2	5	44.7	47.05	49.4	1	64.8	9.3	0.101
P6KE51A	P6KE51A	43.6	5	48.5	51.05	53.6	1	70.1	8.6	0.102
P6KE56A	P6KE56A	47.8	5	53.2	56	58.8	1	77	7.8	0.103
P6KE62A	P6KE62A	53	5	58.9	62	65.1	1	85	7.1	0.104
P6KE68A	P6KE68A	58.1	5	64.6	68	71.4	1	92	6.5	0.104
P6KE75A	P6KE75A	64.1	5	71.3	75.05	78.8	1	103	5.8	0.105
P6KE82A	P6KE82A	70.1	5	77.9	82	86.1	1	113	5.3	0.105
P6KE91A	P6KE91A	77.8	5	86.5	91	95.5	1	125	4.8	0.106
P6KE100A	P6KE100A	85.5	5	95	100	105	1	137	4.4	0.106
P6KE110A	P6KE110A	94	5	105	110.5	116	1	152	4	0.107
P6KE120A	P6KE120A	102	5	114	120	126	1	165	3.6	0.107
P6KE130A	P6KE130A	111	5	124	130.5	137	1	179	3.3	0.107
P6KE150A	P6KE150A	128	5	143	150.5	158	1	207	2.9	0.108
P6KE160A	P6KE160A	136	5	152	160	168	1	219	2.7	0.108
P6KE170A	P6KE170A	145	5	162	170.5	179	1	234	2.6	0.108
P6KE180A	P6KE180A	154	5	171	180	189	1	246	2.4	0.108
P6KE200A	P6KE200A	171	5	190	200	210	1	274	2.2	0.108

3. A transient suppressor is normally selected according to the maximum working peak reverse voltage (V_{RWM}), which should be equal to or greater than the dc or continuous peak operating voltage level.

4. V_{BR} measured at pulse test current I_T at an ambient temperature of 25°C

5. Surge current waveform per Figure 4 and derate per Figures 1 and 2.

6. 1/2 sine wave (or equivalent square wave), PW = 8.3 ms, duty cycle = 4 pulses per minute maximum.



TL074 TL074A - TL074B

LOW NOISE QUAD J-FET OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE $e_n = 15\text{nV}/\sqrt{\text{Hz}}$ (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01% (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : $13\text{V}/\mu\text{s}$ (typ)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The TL074, TL074A and TL074B are high speed J-FET input quad operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

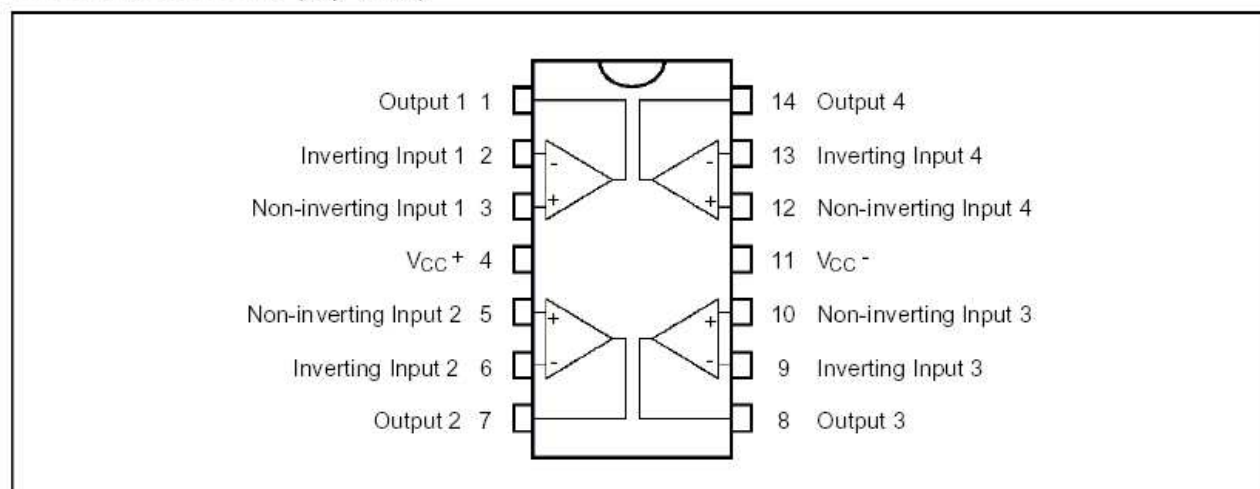
ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TL074M/AM/BM	-55°C, +125°C	•	•
TL074I/AI/BI	-40°C, +105°C	•	•
TL074C/AC/BC	0°C, +70°C	•	•

Example : TL074IN

074-01.TBL

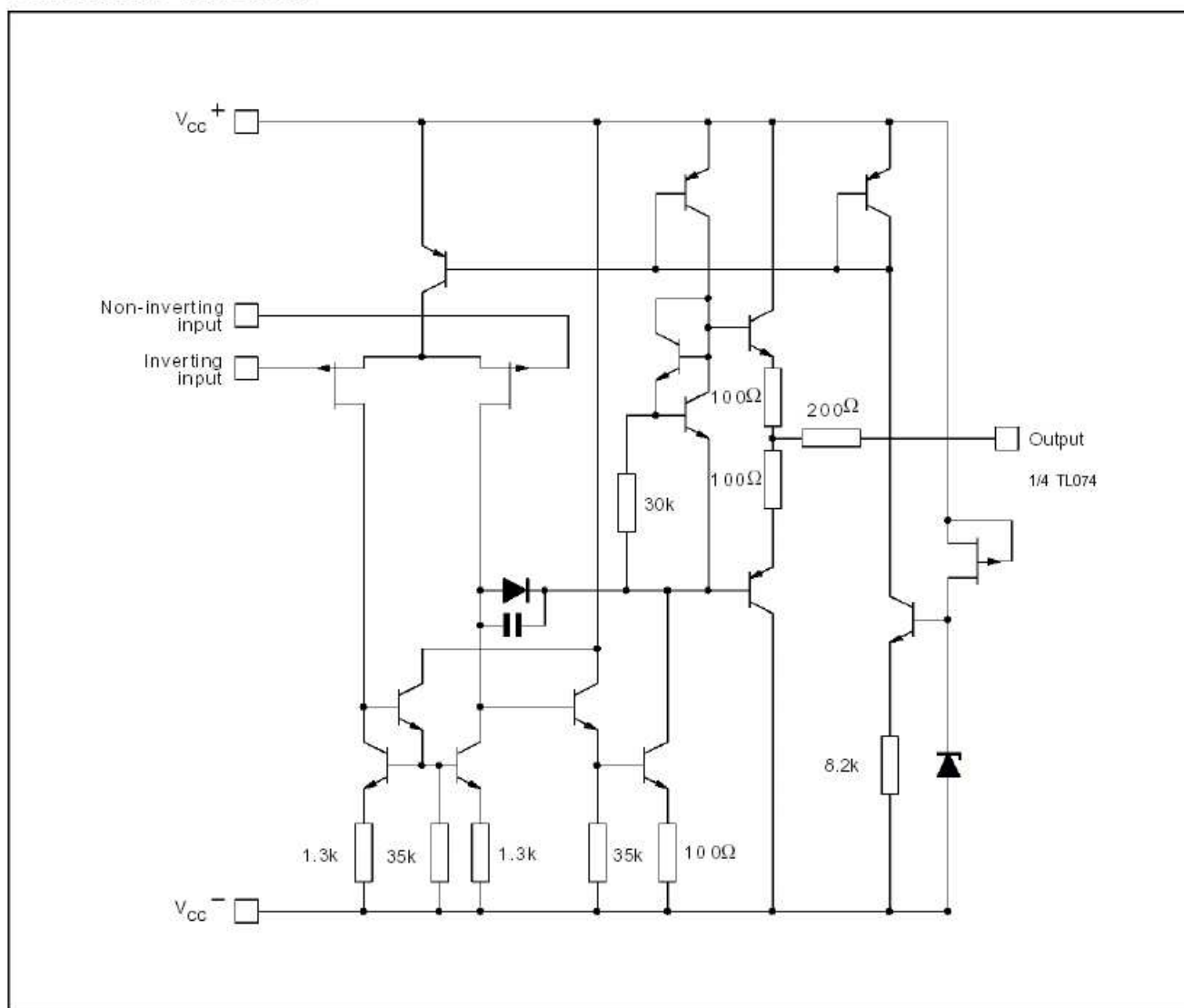
PIN CONNECTIONS (top view)



074-01.EPS

TL074 - TL074A - TL074B

SCHEMATIC DIAGRAM



074-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage - (note 1)	± 18	V
V_i	Input Voltage - (note 3)	± 15	V
V_{id}	Differential Input Voltage - (note 2)	± 30	V
P_{tot}	Power Dissipation	680	mW
	Output Short-circuit Duration - (note 4)	Infinite	
T_{oper}	Operating Free Air Temperature Range	TL074C,AC,BC TL074I,AI,BI TL074M,AM,BM	$^{\circ}\text{C}$

074-02.TBL

Notes :

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^{+} and V_{CC}^{-} .
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and /or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

TL074 - TL074A - TL074B

ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 15V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

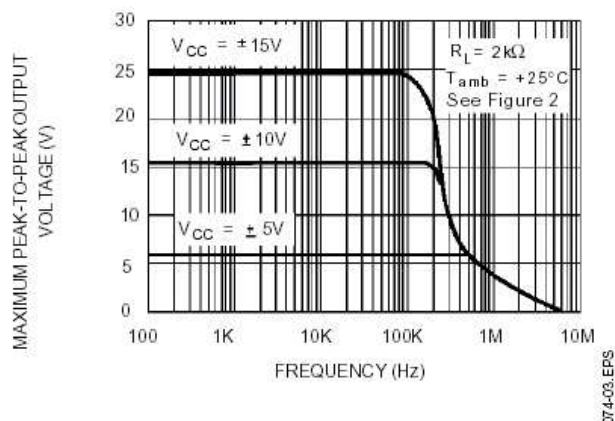
Symbol	Parameter	TL074I,M,AC,AI, AM,BC,BI,BM			TL074C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S = 50\Omega$) $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$ TL074BC,BI,BM TL074BC,BI,BM		3 1	6 3 7 5		3	10 13	mV
DV_{io}	Input Offset Voltage Drift		10			10		$\mu V/^{\circ}C$
I_{io}	Input Offset Current * $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		5	100 4		5	100 10	pA nA
I_{ib}	Input Bias Current * $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		20	200 20		30	200 20	pA nA
A_{vd}	Large Signal Voltage Gain ($R_L = 2k\Omega$, $V_O = \pm 10V$) $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	200		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S = 50\Omega$) $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	86		70 70	86		dB
I_{cc}	Supply Current, per Amp, no Load $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input Common Mode Voltage Range	± 11	+15 -12		± 11	+15 -12		V
CMR	Common Mode Rejection Ratio ($R_S = 50\Omega$) $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	80 80	86		70 70	86		dB
I_{os}	Output Short-circuit Current $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{opp}$	Output Voltage Swing $T_{amb} = 25^{\circ}C$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 2k\Omega$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 10k\Omega$	10 12 10 12	12 13.5		10 12 10 12	12 13.5		V
SR	Slew Rate ($V_{in} = 10V$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^{\circ}C$, unity gain)	8	13		8	13		V/ μs
t_r	Rise Time ($V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^{\circ}C$, unity gain)		0.1			0.1		μs
Kov	Overshoot ($V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^{\circ}C$, unity gain)		10			10		%
GBP	Gain Bandwidth Product ($f = 100kHz$, $T_{amb} = 25^{\circ}C$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$)	2	3		2	3		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
THD	Total Harmonic Distortion ($f = 1kHz$, $A_V = 20dB$, $R_L = 2k\Omega$, $C_L = 100pF$, $T_{amb} = 25^{\circ}C$, $V_O = 2V_{PP}$)		0.01			0.01		%
e_n	Equivalent Input Noise Voltage ($f = 1kHz$, $R_S = 100\Omega$)		15			15		$\frac{nV}{\sqrt{Hz}}$
ϕ_m	Phase Margin		45			45		Degrees
V_{O1}/V_{O2}	Channel Separation ($A_V = 100$)		120			120		dB

074-03.TBL

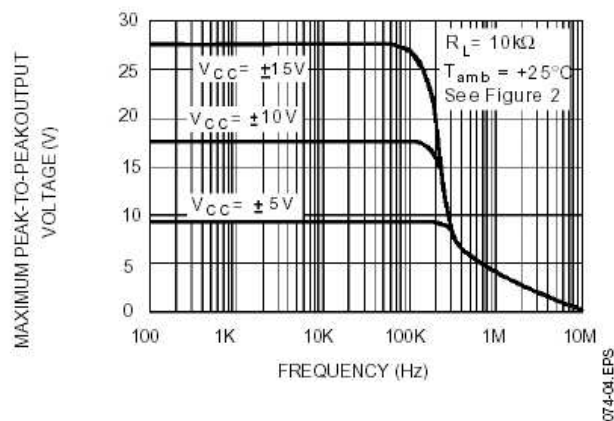
* The input bias currents are junction leakage currents which approximately double for every $10^{\circ}C$ increase in the junction temperature.

TL074 - TL074A - TL074B

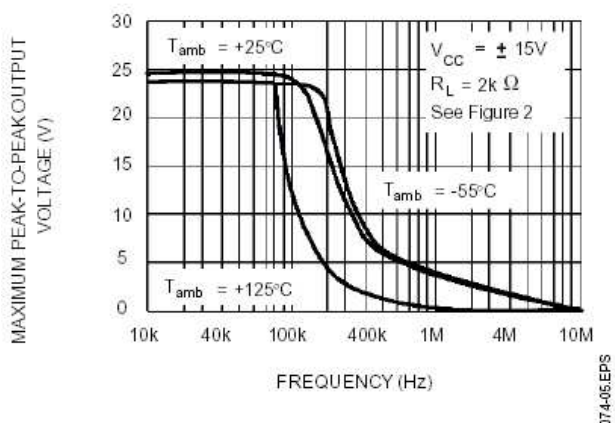
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



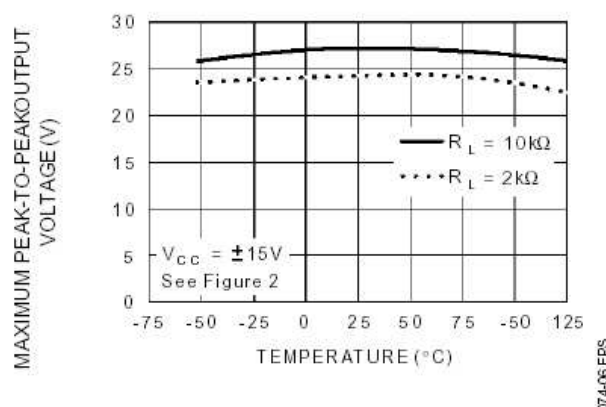
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



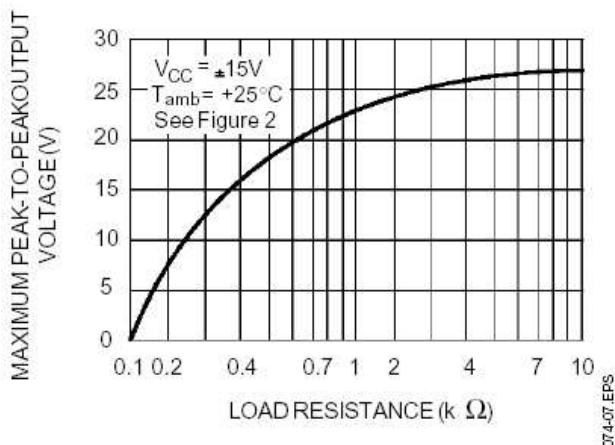
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREQUENCY



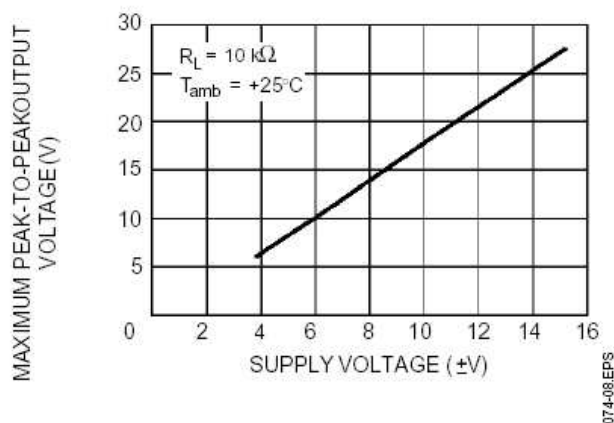
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS FREE AIR TEMP.



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE



TLE206x, TLE206xA, TLE206xB, TLE206xY EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μ POWER OPERATIONAL AMPLIFIERS

SLOS193A – FEBRUARY 1997 – REVISED MARCH 1998

- 2× Bandwidth (2 MHz) of the TL06x and TL03x Operational Amplifiers
- Low Supply Current . . . 290 μ A/Ch Typ
- On-chip Offset Voltage Trimming for Improved DC Performance
- High Output Drive, Specified into 100- Ω Loads
- Lower Noise Floor Than Earlier Generations of Low-Power BiFETs

description

The TLE206x series of low-power JFET-input operational amplifiers doubles the bandwidth of the earlier generation TL06x and TL03x BiFET families without significantly increasing power consumption. Texas Instruments Excalibur process also delivers a lower noise floor than the TL06x and TL03x. On-chip zener trimming of offset voltage yields precision grades for dc-coupled applications. The TL206x devices are pin-compatible with other TI BiFETs; they can be used to double the bandwidth of TL06x and TL03x circuits, or to reduce power consumption of TL05x, TL07x, and TL08x circuits by nearly 90%.

BiFET operational amplifiers offer the inherently-higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. This makes them better suited for interfacing with high-impedance sensors or very low-level ac signals. They also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption. The TLE206x family features a high-output-drive circuit capable of driving 100- Ω loads at supplies as low as ± 5 V. This makes them uniquely suited for driving transformer loads in modems and other applications requiring good ac characteristics, low power, and high output drive.

Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required and loads should be terminated to a virtual ground node at mid-supply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

The TLE206x are fully specified at ± 15 V and ± 5 V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC- and TLV-prefixes) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to slew rate and bandwidth requirements, and output loading. The Texas Instrument TLV2432 and TLV2442 CMOS operational amplifiers are excellent choices to consider.

TLE2062 AVAILABLE OPTIONS

PACKAGED DEVICES						CHIP FORM [‡] (Y)
T _A	V _{IO} max AT 25°C	SMALL OUTLINE [†] (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	1 mV 2 mV 4 mV	TLE2062BCD TLE2062ACD TLE2062CD	— — —	— — —	TLE2062BCP TLE2062ACP TLE2062CP	— — TLE2062Y
–40°C to 85°C	1 mV 2 mV 4 mV	TLE2062BID TLE2062AID TLE2062ID	— — —	— — —	TLE2062BIP TLE2062AIP TLE2062IP	— — —
–55°C to 125°C	1 mV 2 mV 4 mV	TLE2062BMD TLE2062AMD TLE2062MD	TLE2062BMFK TLE2062AMFK TLE2062MFK	TLE2062BMJG TLE2062AMJG TLE2062MJG	TLE2062BMP TLE2062AMP TLE2062MP	— — —

[†] The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2062ACDR).

[‡] Chip forms are tested at 25°C only.

TLE206x, TLE206xA, TLE206xB, TLE206xY EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC+} (see Note 1)	19 V
Supply voltage, V_{CC-}	–19 V
Differential input voltage, V_{ID} (see Note 2)	±38 V
Input voltage range, V_I (any input)	± V_{CC}
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+}	80 mA
Total current out of V_{CC-}	–80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
2. Differential voltages are at $IN+$ with respect to $IN-$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	±3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5\text{ V}$	–1.6	4	–1.6	4	–1.6	4	V
	$V_{CC\pm} = \pm 15\text{ V}$	–11	13	–11	13	–11	13	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

TLE206x, TLE206xA, TLE206xB, TLE206xY
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE
 μ POWER OPERATIONAL AMPLIFIERS

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TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2062C TLE2062AC TLE2062BC			UNIT
				MIN	TYP	MAX	
V _{IO} Input offset voltage	TLE2062C	V _{IC} = 0, R _S = 50 Ω	25°C	1	5	mV	
			Full range	5.9			
	TLE2062AC		25°C	0.9	4		
			Full range	4.9			
	TLE2062BC		25°C	0.7	3		
			Full range	3.9			
α _{VIO} Temperature coefficient of input offset voltage			Full range	6		μV/°C	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo	
I _{IO} Input offset current			25°C	1		pA	
			Full range	0.8		nA	
I _{IB} Input bias current			25°C	3		pA	
			Full range	2		nA	
V _{ICR} Common-mode input voltage range		25°C	−1.6 to 4	−2 to 6		V	
		Full range	−1.6 to 4			V	
V _{OM+} Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	3.5	3.7	V		
		Full range	3.3				
	R _L = 100 Ω	25°C	2.5	3.1			
		Full range	2				
V _{OM−} Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	−3.7	−3.9	V		
		Full range	−3.3				
	R _L = 100 Ω	25°C	−2.5	−2.7			
		Full range	−2				
A _{VD} Large-signal differential voltage amplification	V _O = ± 2.8 V, R _L = 10 kΩ	25°C	15	80	V/mV		
		Full range	2				
	V _O = 0 to 2 V, R _L = 100 Ω	25°C	0.75	45			
		Full range	0.5				
	V _O = 0 to −2 V, R _L = 100 Ω	25°C	0.5	3			
		Full range	0.25				
r _i Input resistance		25°C	10 ¹²		Ω		
c _i Input capacitance		25°C	4		pF		
z _o Open-loop output impedance	I _O = 0	25°C	560		Ω		
CMRR Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	65	82	dB		
		Full range	65				
k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ± 5 V to ± 15 V, R _S = 50 Ω	25°C	75	93	dB		
		Full range	75				

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE206x, TLE206xA, TLE206xB, TLE206xY
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE
μPOWER OPERATIONAL AMPLIFIERS
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TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2062C TLE2062AC TLE2062BC			UNIT
			MIN	TYP	MAX	
I_{CC} Supply current	$V_O = 0$, No load	25°C		560	620	μA
		Full range			635	
ΔI_{CC} Supply-current change over operating temperature range		Full range		26		μA

† Full range is 0°C to 70°C.

TLE2062C operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2062C TLE2062AC TLE2062BC			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain (see Figure 1)	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	2.2	3.4		$\text{V}/\mu\text{s}$
		Full range	2.1			
V_n Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$, $R_S = 20\text{ }\Omega$	25°C		59	100	$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$	25°C		43	60	
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		μV
I_n Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1		$\text{fA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$, $A_{VD} = 2$, $f = 10\text{ kHz}$	25°C		0.025%		
B_1 Unity-gain bandwidth (see Figure 3)	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		1.8		MHz
	$R_L = 100\text{ }\Omega$, $C_L = 100\text{ pF}$	25°C		1.3		
Settling time	0.1%	25°C		5		μs
	0.01%	25°C		10		
B_{OM} Maximum output-swing bandwidth	$A_{VD} = 1$, $R_L = 10\text{ k}\Omega$	25°C		140		kHz
ϕ_m Phase margin at unity gain (see Figure 3)	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		58°		
	$R_L = 100\text{ }\Omega$, $C_L = 100\text{ pF}$	25°C		75°		

† Full range is 0°C to 70°C.

TLE206x, TLE206xA, TLE206xB, TLE206xY
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE
μPOWER OPERATIONAL AMPLIFIERS

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TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2062C TLE2062AC TLE2062BC			UNIT
				MIN	TYP	MAX	
V _{IO} Input offset voltage	TLE2062C	V _{IC} = 0, R _S = 50 Ω	25°C	0.9 4		mV	
	TLE2062AC		Full range	4.9			
			25°C	0.8 2			
			Full range	2.9			
			25°C	0.5 1			
	TLE2062BC		Full range	1.9			
α _{VIO} Temperature coefficient of input offset voltage			Full range	6		μV/°C	
Input offset voltage long-term drift (see Note 4)			25°C	0.04		μV/mo	
I _{IO} Input offset current			25°C	2		pA	
	I _{IB} Input bias current		Full range	1		nA	
			25°C	4		pA	
			Full range	3		nA	
V _{ICR} Common-mode input voltage range		25°C	–11 to 13	–12 to 16	V		
		Full range	–11 to 13		V		
V _{OM+} Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	13.2	13.7	V		
		Full range	13				
	R _L = 600 Ω	25°C	12.5	13.2			
		Full range	12				
V _{OM–} Maximum negative peak output voltage swing	R _L = 10 kΩ	25°C	–13.2	–13.7	V		
		Full range	–13				
	R _L = 600 Ω	25°C	–12.5	–13			
		Full range	–12				
A _{VD} Large-signal differential voltage amplification	V _O = ± 10 V, R _L = 10 kΩ	25°C	30	230	V/mV		
		Full range	20				
	V _O = 0 to 8 V, R _L = 600 Ω	25°C	25	100			
		Full range	10				
	V _O = 0 to –8 V, R _L = 600 Ω	25°C	3	25			
		Full range	1				
r _i Input resistance		25°C	10 ¹²		Ω		
c _i Input capacitance		25°C	4		pF		
z _O Open-loop output impedance	I _O = 0	25°C	560		Ω		
CMRR Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	72	90	dB		
		Full range	70				
k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ± 5 V to ± 15 V, R _S = 50 Ω	25°C	75	93	dB		
		Full range	75				

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE206x, TLE206xA, TLE206xB, TLE206xY
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE
μPOWER OPERATIONAL AMPLIFIERS

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TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2062C TLE2062AC TLE2062BC			UNIT
			MIN	TYP	MAX	
I_{CC} Supply current	$V_O = 0\text{ V}$, No load	25°C		625	690	μA
		Full range			715	
ΔI_{CC} Supply-current change over operating temperature range		Full range		36		μA

† Full range is 0°C to 70°C.

TLE2062C operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2062C TLE2062AC TLE2062BC			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain (see Figure 1)	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	2.6	3.4		$\text{V}/\mu\text{s}$
		Full range	2.5			
V_n Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$, $R_S = 20\text{ }\Omega$	25°C		70	100	$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$	25°C		40	60	
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1		μV
I_n Equivalent input noise current	$f = 1\text{ kHz}$	25°C		1.1		$\text{fA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$, $A_{VD} = 2$, $f = 10\text{ kHz}$	25°C		0.025%		
B_1 Unity-gain bandwidth (see Figure 3)	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		2		MHz
	$R_L = 600\text{ }\Omega$, $C_L = 100\text{ pF}$	25°C		1.5		
Settling time	0.1%	25°C		5		μs
	0.01%	25°C		10		
B_{OM} Maximum output-swing bandwidth	$A_{VD} = 1$, $R_L = 10\text{ k}\Omega$	25°C		40		kHz
ϕ_m Phase margin at unity gain (see Figure 3)	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		60°		
	$R_L = 600\text{ }\Omega$, $C_L = 100\text{ pF}$	25°C		70°		

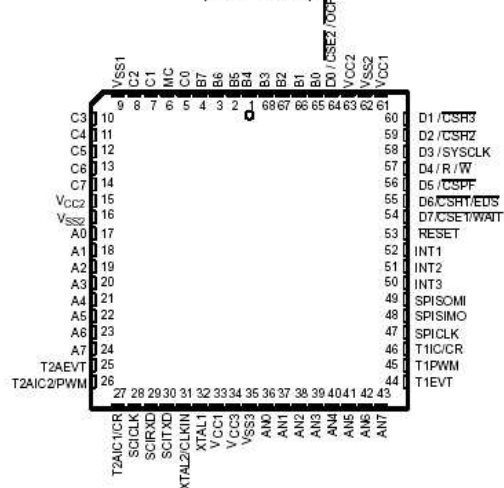
† Full range is 0°C to 70°C.

TMS370Cx5x 8-BIT MICROCONTROLLER

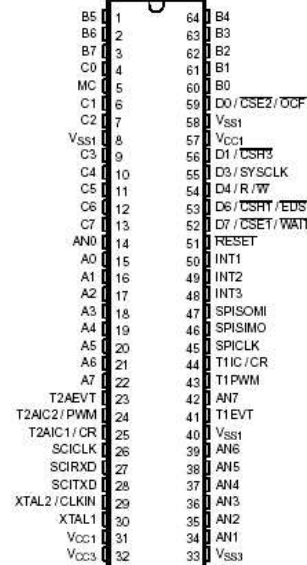
SPNS010F – DECEMBER 1986 – REVISED FEBRUARY 1997

- CMOS/EEPROM/EPROM Technologies on a Single Device
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- Internal System Memory Configurations
 - On-Chip Program Memory Versions
 - ROM: 4K to 48K Bytes
 - EPROM: 16K to 48K Bytes
 - ROM-less
 - Data EEPROM: 256 or 512 Bytes
 - Static RAM: 256 to 3.5K Bytes
 - External Memory/Peripheral Wait States
 - Precoded External Chip-Select Outputs in Microcomputer Mode
- Flexible Operating Features
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)
 - Divide-by-1 (2 MHz – 5 MHz SYSCLK)
 - Phase-Locked Loop (PLL)
 - Supply Voltage (V_{CC}): 5 V $\pm$ 10%
- Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)
- Two 16-Bit General-Purpose Timers
- On-Chip 24-Bit Watchdog Timer
- Two Communication Modules
 - Serial Communications Interface 1 (SCI1)
 - Serial Peripheral Interface (SPI)
- Flexible Interrupt Handling
- TMS370 Series Compatibility
- CMOS/Package/TTL-Compatible I/O Pins
 - 64-Pin Plastic and Ceramic Shrink Dual-In-Line Packages/44 Bidirectional, 9 Input Pins
 - 68-Pin Plastic and Ceramic Leaded Chip Carrier Packages/46 Bidirectional, 9 Input Pins
 - All Peripheral Function Pins Are Software Configurable for Digital I/O

FN/FZ PACKAGE
(TOP VIEW)



JN/NM PACKAGE
(TOP VIEW)



- Workstation/PC-Based Development System
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer



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**TEXAS
INSTRUMENTS**

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TMS370Cx5x 8-BIT MICROCONTROLLER

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Pin Descriptions

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	SDIP (64)	LCC (68)		
A0 A1 A2 A3 A4 A5 A6 A7	DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	15 16 17 18 19 20 21 22	17 18 19 20 21 22 23 24	I/O	Single-chip mode: Port A is a general-purpose bidirectional I/O port. Expansion mode: Port A can be individually programmed as the external bidirectional data bus (DATA0–DATA7).
B0 B1 B2 B3 B4 B5 B6 B7	ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7	60 61 62 63 64 1 2 3	65 66 67 68 1 2 3 4	I/O	Single-chip mode: Port B is a general-purpose bidirectional I/O port. Expansion mode: Port B can be individually programmed as the low-order address output bus (ADDR0–ADDR7).
C0 C1 C2 C3 C4 C5 C6 C7	ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15	4 6 7 9 10 11 12 13	5 7 8 10 11 12 13 14	I/O	Single-chip mode: Port C is a general-purpose bidirectional I/O port. Expansion mode: Port C can be individually programmed as the high-order address output bus (ADDR8–ADDR15).
INT1 INT2 INT3	NMI — —	50 49 48	52 51 50	I I/O I/O	External (nonmaskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	E0 E1 E2 E3 E4 E5 E6 E7	14 34 35 36 37 38 39 42	36 37 38 39 40 41 42 43	I	ADC1 analog input (AN0–AN7) or positive reference pins (AN1–AN7) Port E can be individually programmed as general-purpose input pins if not used as ADC1 analog input or positive reference input.
VCC3 VSS3		32 33	34 35		ADC1 positive-supply voltage and optional positive-reference input pin ADC1 ground reference pin
RESET		51	53	I/O	System reset bidirectional pin. RESET, as an input, initializes the microcontroller; as open-drain output, RESET indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC		5	6	I	Mode control (MC) pin. MC enables EEPROM write-protection override (WPO) mode, also EPROM Vpp.
XTAL2/CLKIN XTAL1		29 30	31 32	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
VCC1		31, 57	33, 61		Positive supply voltage
VCC2		—	15, 63		Positive supply voltage

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.



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TMS370Cx5x 8-BIT MICROCONTROLLER

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Pin Descriptions (Continued)

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	SDIP (64)	LCC (68)		
VSS1		8, 58,40	9		Ground reference for digital logic
VSS2		—	16,62		Ground reference for digital I/O logic
D0 D1 D2 D3 D4 D5 D6 D7	FUNCTION				Single-chip mode: Port D is a general-purpose bidirectional I/O port. Each of the port D pins can be individually configured as a general-purpose I/O pin, primary memory control signal (function A), or secondary memory control signal (function B). All chip selects are independent and can be used for memory bank switching. Refer to Table 1 for function A memory accesses. I/O pin A: Chip select eighth output 2 goes low during memory accesses I/O pin B: Opcode fetch goes low during the opcode fetch memory cycle. I/O pin A: Chip select half output 3 goes low during memory accesses. I/O pin B: Reserved I/O pin A: Chip select half output 2 goes low during memory accesses. I/O pin B: Reserved I/O pin A, B: Internal clock signal is 1/1 (PLL) or 1/4 XTAL2/CLKIN frequency. I/O pin A, B: Read/write output pin I/O pin A: Chip select peripheral output for peripheral file goes low during memory accesses. I/O pin B: Reserved I/O pin A: Chip select half output 1 goes low during memory accesses. I/O pin B: External data strobe output goes low during memory accesses from external memory and has the same timings as the five chip selects. I/O pin A: Chip select eighth output goes low during memory accesses. I/O pin B: Wait input pin extends bus signals.
	A	B			
	$\overline{\text{CSE2}}$	$\overline{\text{OCF}}$	59	64	
	$\overline{\text{CSH3}}$	—	56	60	
	$\overline{\text{CSH2}}$	—	—	59	
	SYSCLK	SYSCLK	55	58	
	R/ $\overline{\text{W}}$	R/ $\overline{\text{W}}$	54	57	
	$\overline{\text{CSPF}}$	—	—	56	
	$\overline{\text{CSH1}}$	$\overline{\text{EDS}}$	53	55	
	$\overline{\text{CSE1}}$	$\overline{\text{WAIT}}$	52	54	
SCITXD SCIRXD SCICLK	SCII01 SCII02 SCII03	28 27 26	30 29 28	I/O	SCI transmit data output pin/general-purpose bidirectional pin (see Note 1) SCI receive data input pin/general-purpose bidirectional pin SCI bidirectional serial clock pin/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	T1IO1 T1IO2 T1IO3	44 43 41	46 45 44	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin Timer1 pulse-width-modulation (PWM) output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
T2AIC1/CR T2AIC2/PWM T2AEVT	T2AIO1 T2AIO2 T2AIO3	25 24 23	27 26 25	I/O	Timer2A input capture 1/counter reset input pin/general-purpose bidirectional pin Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin Timer2A external event input pin/general-purpose bidirectional pin
SPISOMI SPISIMO SPICLK	SPIIO1 SPIIO2 SPIIO3	47 46 45	49 48 47	I/O	SPI slave output pin, master input pin/general-purpose bidirectional pin SPI slave input pin, master output pin/general-purpose bidirectional pin SPI bidirectional serial clock pin/general-purpose bidirectional pin

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Port D3 also can be configured as SYSCLK.

NOTE 1: The three-pin configuration SCI is referred to as SCI1.

Table 1. Function A: Memory Accesses Locations for 'x5x Devices

FUNCTION A	'X50, 'X52, 'X53, AND 'X56	'X58	'X59
$\overline{\text{CSEx}}$	2000h – 3FFFh (8K bytes)	A000h – BFFFh (8K bytes)	E000h – EFFFh (4K bytes)
$\overline{\text{CSHx}}$	8000h – FFFFh (32K bytes)	C000h – FFFFh (16K bytes)	F000h – FFFFh (4K bytes)
$\overline{\text{CSPF}}$	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)



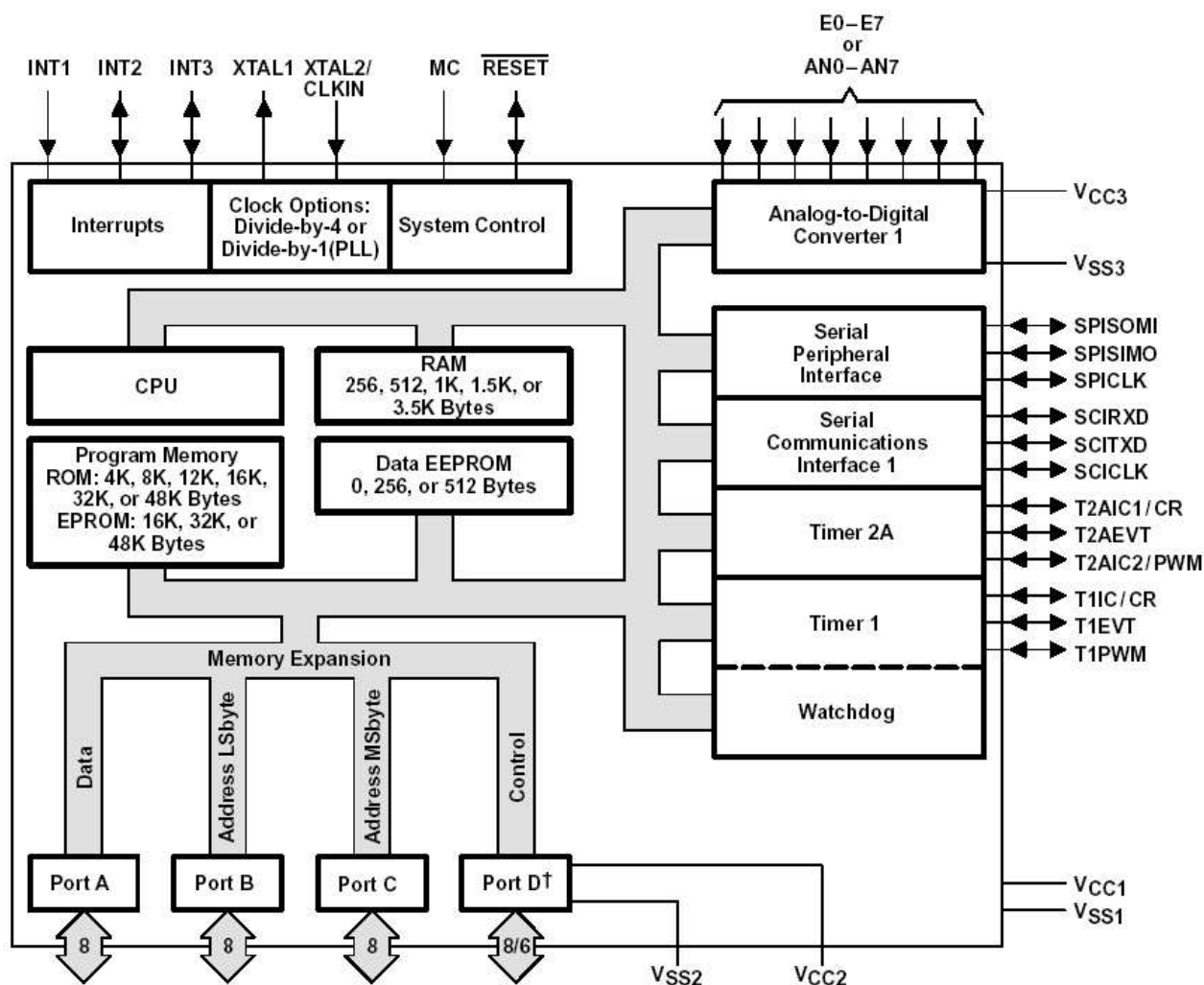
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functional block diagram



† For the 64-pin devices, there are only six pins for port D.

description

The TMS370Cx5x family of single-chip 8-bit microcontrollers provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations. The TMS370Cx5x family presently consists of twenty-one devices which are grouped into seven main sub-families: the TMS370Cx50, TMS370Cx52, TMS370Cx53, TMS370Cx56, TMS370Cx58, TMS370Cx59, and SE370C75x.

The TMS370Cx5x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions, make the TMS370Cx5x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application. Table 2 provides a memory configuration overview of the TMS370Cx5x devices.

TMS370Cx5x

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description (continued)

Table 2. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXP. (BYTES)	DATA MEMORY (BYTES)		OPERATING MODES		PACKAGES 68 PIN PLCC/CLCC, OR 64 PIN PSDIP/CSDIP
	ROM	EPROM		RAM	EEPROM	μC†	μP†	
TMS370Cx50: TMS370C050, TMS370C150, TMS370C250, AND TMS370C350								
TMS370C050A	4K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C150A	—	—	56K	256	—	—	√	FN – PLCC
TMS370C250A	—	—	56K	256	256	—	√	FN – PLCC
TMS370C350A	4K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370Cx52: TMS370C052, TMS370C352, AND TMS370C452								
TMS370C052A	8K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C352A	8K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370C452A†	8K	—	112K	256	256	√	√	FN – PLCC
TMS370Cx53: TMS370C353								
TMS370C353A	12K	—	112K	1.5K	—	√	√	FN – PLCC
TMS370Cx56: TMS370C056, TMS370C156, TMS370C256, TMS370C356, TMS370C456, AND TMS370C756								
TMS370C056A	16K	—	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370C156A	—	—	56K	512	—	—	√	FN – PLCC
TMS370C256A	—	—	56K	512	512	—	√	FN – PLCC
TMS370C356A	16K	—	112K	512	—	√	√	FN – PLCC / NM –PSDIP
TMS370C456A†	16K	—	112K	512	512	√	√	FN – PLCC
TMS370C756A	—	16K	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370Cx58: TMS370C058, TMS370C358, AND TMS370C758								
TMS370C058A	32K	—	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370C358A	32K	—	64K	1K	—	√	√	FN – PLCC / NM –PSDIP
TMS370C758A, TMS370C758B	—	32K	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370Cx59: TMS370C059 AND TMS370C759								
TMS370C059A§	48K	—	20K	3.5K	256	√	√	FN – PLCC
TMS370C759A§	—	48K	20K	3.5K	256	√	√	FN – PLCC
EPROM DEVICE: SE370C756, SE370C758, and SE370C759								
SE370C756A¶	—	16K	112K	512	512	√	√	FZ – CLCC / JN –CSDIP
SE370C758A¶, SE370C758B¶	—	32K	64K	1K	256	√	√	FZ – CLCC / JN –CSDIP
SE370C759A¶	—	48K	20K	3.5K	256	√	√	FZ – CLCC

† μC – Microcomputer mode

‡ μP – Microprocessor mode

§ TMS370C45x support ROM memory security. Refer to the program ROM section.

¶ Only operate up to 3 MHz SYSCLK

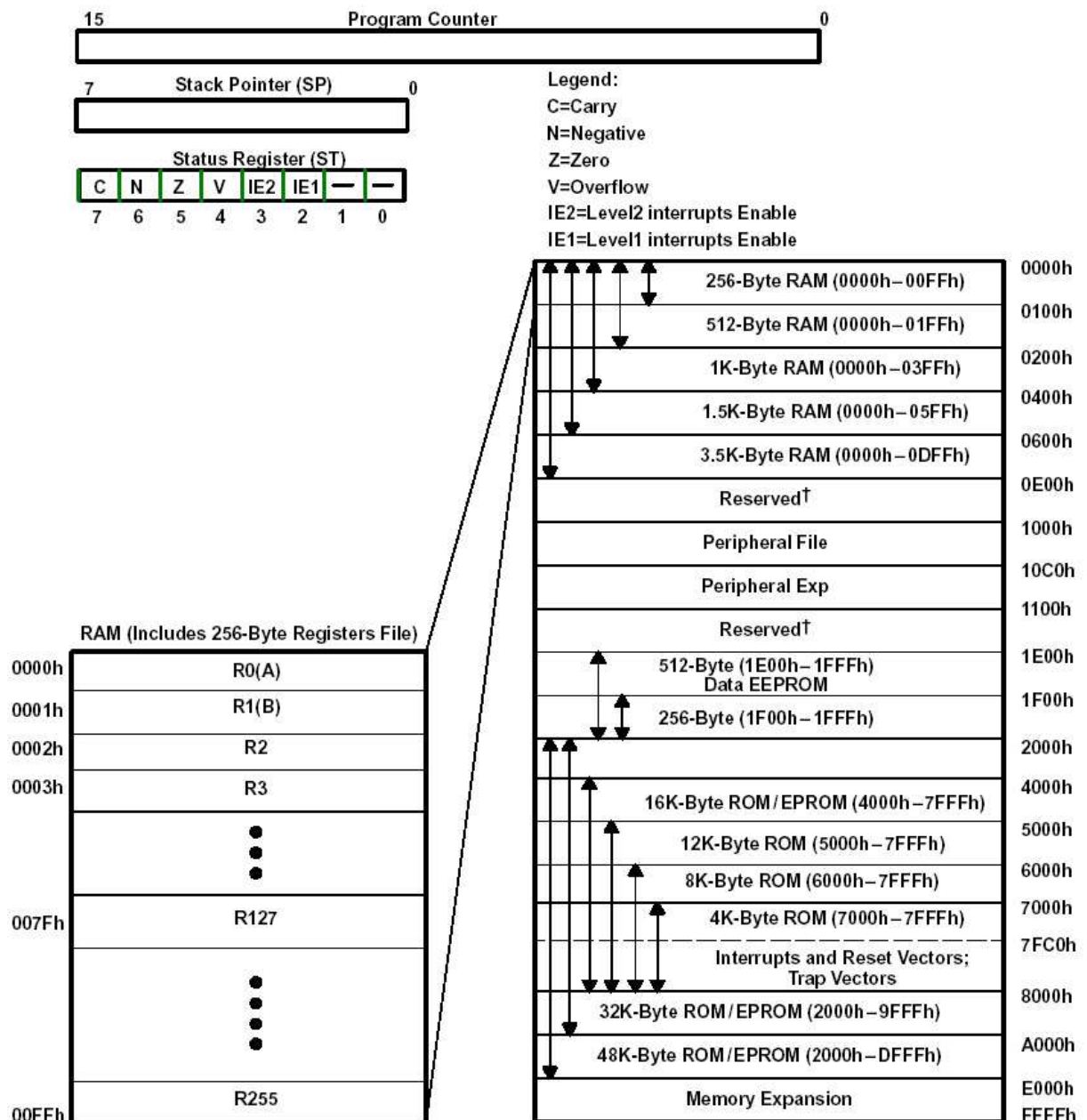
¶ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

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CPU

The CPU used on TMS370Cx5x devices is the high-performance 8-bit TMS370 CPU module. The 'x' implements an efficient register-to-register architecture that eliminates the conventional accumula bottleneck. The complete 'x5x' instruction set is summarized in Table 23. Figure 1 illustrates the CPU regist and memory blocks.



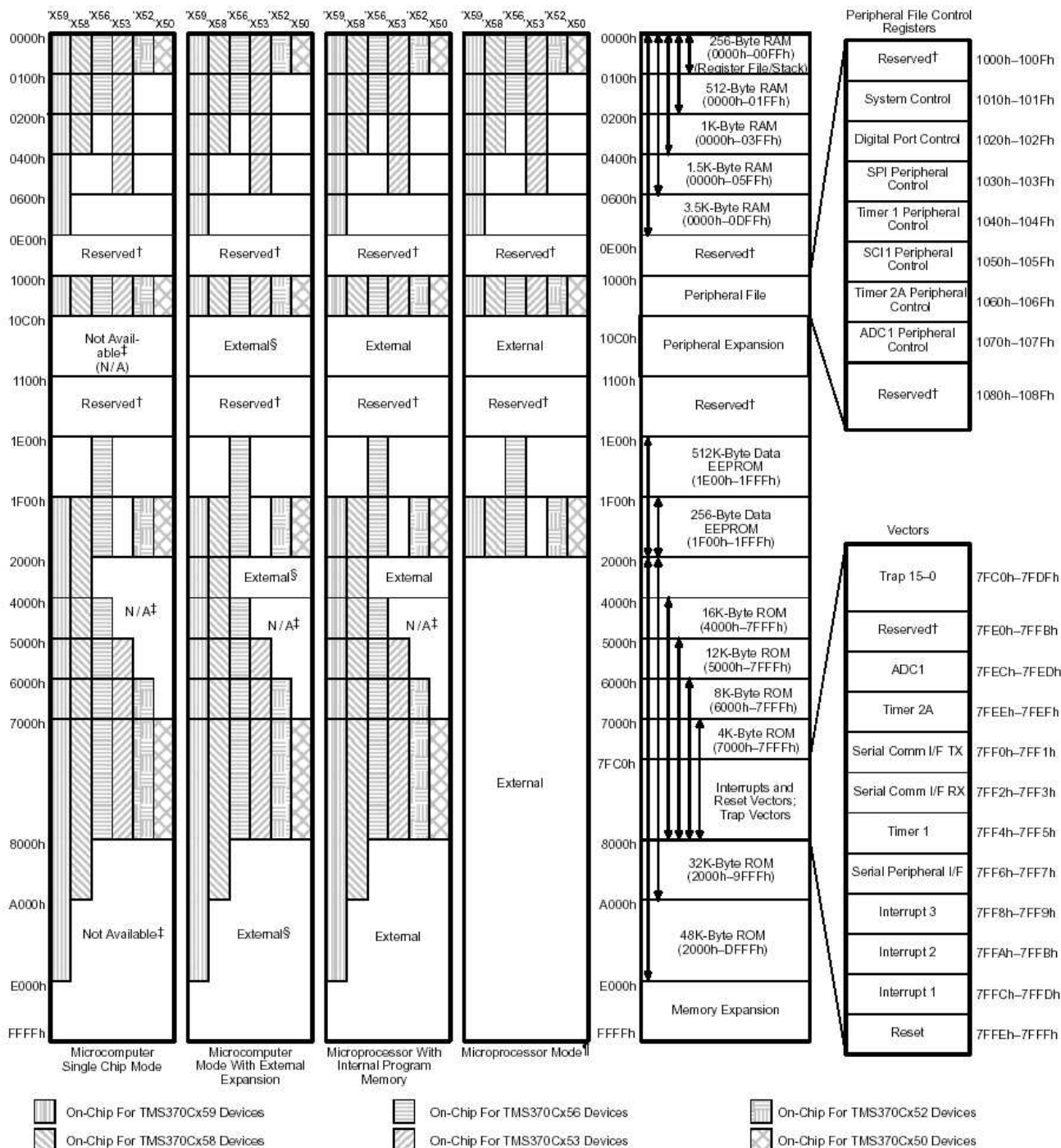
† Reserved means the address space is reserved for future expansion.

Figure 1. Programmer's Model

TMS370Cx5x 8-BIT MICROCONTROLLER

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memory map (continued)



† Reserved = the address space is reserved for future expansion.

‡ Not available (N/A) = address space unavailable in the mode illustrated.

§ Precoded chip select outputs available on external expansion bus.

¶ Microprocessor mode is designed for ROM-less devices ('x50 and 'x56). ROM and EPROM devices can also be used in this mode but all on-chip memory is ignored.

Figure 3. TMS370Cx5x Memory Map

TMS370Cx5x 8-BIT MICROCONTROLLER

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interrupts (continued)

Table 12. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY†
External RESET Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET‡	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1‡	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2‡	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3‡	7FF8h, 7FF9h	4
SPI RX/TX complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT§	7FF4h, 7FF5h	6
SCI RX data register full SCI RX break detect	RXRDY FLAG BRKDT FLAG	RXINT‡	7FF2h, 7FF3h	7
SCI TX data register empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	8
Timer 2A overflow Timer 2A compare 1 Timer 2A compare 2 Timer 2A external edge Timer 2A input capture 1 Timer 2A input capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	9
A/D conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	10

† Relative priority within an interrupt level

‡ Releases microcontroller from STANDBY and HALT low-power modes.

§ Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx5x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx5x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to 1 to enter the nonprivileged mode; disabling write operations to specific configuration control bits within the peripheral file. Table 13 displays the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

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instruction set overview

Table 23 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370Cx5x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 23. TMS370 Family Opcode/Instruction Map† (Continued)

MSN															
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
JNV ra 2/5	MPY Rs,A 2/4/6	MPY #n,A 2/4/5	MPY Rs,B 2/4/6	MPY Rs,Rd 3/4/8	MPY #n,B 2/4/5	MPY B,A 1/4/7	MPY #n,Rd 3/4/7	BR lAb 3/9	BR *Rp 2/8	BR *lAb[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP lAb & lAb,A 3/11	CMP *Rp,A 2/10	CMP *lAb[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 2 1/7
JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lAb 3/13	CALL *Rp 2/12	CALL *lAb[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lAb 3/15	CALLR *Rp 2/14	CALLR *lAb[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx)

MOVW *r[Rn] 4/15	8	F4	MOVW *r[Rn],A 4/17	DIV Rn,A 3/14+63
JMPL *r[Rn] 4/16	9	F4	JMPL *r[Rn] 4/16	
MOV *r[Rn],A 4/17	A	F4	MOV A,*r[Rn] 4/16	
BR *r[Rn] 4/16	C	F4	BR *r[Rn] 4/16	
CMP *r[Rn],A 4/18	D	F4	CMP *r[Rn],A 4/18	
CALL *r[Rn] 4/20	E	F4	CALL *r[Rn] 4/20	
CALLR *r[Rn] 4/22	F	F4	CALLR *r[Rn] 4/22	

Legend

- * - Indirect addressing operand prefix
- & - Direct addressing operand prefix
- # - Immediate operand
- #16 - Immediate 16-bit number
- lAb - 16-label
- n - Immediate 8-bit number
- Pd - Peripheral register containing destination type
- Pn - Peripheral register
- Ps - Peripheral register containing source byte
- ra - Relative address
- Rd - Register containing destination type
- Rn - Register file
- Rp - Register pair
- Rpd - Destination register pair
- Rps - Source Register pair
- Rs - Register containing source byte

† All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, $V_{CC1}^{\ddagger}$, V_{CC2} , V_{CC3} (see Note 2)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC1}) [§]	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] $V_{CC1} = V_{CC}$

[§] Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 2: Unless otherwise noted, all voltage values are with respect to V_{SS1} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 2)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)	3		5.5	
V_{CC2}	Digital I/O supply voltage (see Note 2)	4.5	5	5.5	V
V_{CC3}	Analog supply voltage (see Note 2)	4.5	5	5.5	
V_{SS2}	Digital I/O supply ground	–0.3	0	0.3	V
V_{SS3}	Analog supply ground	–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		0.8	V
		MC, normal operation		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		V_{CC1}	V
		MC (non-WPO mode)		$V_{CC1} - 0.3$ to $V_{CC1} + 0.3$	
		XTAL2/CLKIN		$0.8 V_{CC1}$ to V_{CC1}	
		RESET		$0.7 V_{CC1}$ to V_{CC1}	
V_{MC}	MC (mode control) voltage (see Note 4)	EEPROM write protect override (WPO)		11.7 to 13	V
		EPROM programming voltage (V_{pp})		13 to 13.5	
		Microprocessor		$V_{CC1} - 0.3$ to $V_{CC1} + 0.3$	
		Microcomputer		V_{SS1} to 0.3	
T_A	Operating free-air temperature	L version		0 to 70	°C
		A version		–40 to 85	
		T version		–40 to 105	

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

3. RESET must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.

4. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system-clock cycles (t_C) before RESET goes inactive (high). The WPO mode can be selected anytime a sufficient voltage is present on MC.

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otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage (see Note 5)		I _{OL} = 1.4 mA				0.4	V
V _{OH}	High-level output voltage		I _{OH} = −50 μA		0.9 V _{CC1}		V	
			I _{OH} = −2 mA		2.4			
I _I	Input current	MC	0 V < V _I ≤ 0.3 V				10	μA
			0.3 V < V _I < V _{CC1} − 0.3 V				50	
			V _{CC1} − 0.3 V ≤ V _I ≤ V _{CC1} + 0.3 V				10	
			V _{CC1} + 0.3 V < V _I ≤ 13 V				650	
			12 V ≤ V _I ≤ 13 V		See Note 6			50
		I/O pins		0 V ≤ V _I ≤ V _{CC1}				± 10
I _{OL}	Low-level output current (see Note 5)		V _{OL} = 0.4 V			1.4		mA
I _{OH}	High-level output current		V _{OH} = 0.9 V _{CC1}			− 50		μA
			V _{OH} = 2.4 V			− 2		mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 9)	TMS370Cx50A TMS370Cx52A	SYSCLK = 5 MHz	See Notes 7 and 8		30	45	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				35	56	
		TMS370Cx50A TMS370Cx52A	SYSCLK = 3 MHz	See Notes 7 and 8		20	30	
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				25	36	
		TMS370Cx59A†				46	55	
	Supply current (operating mode) OSC POWER bit = 0 (see Note 9)	TMS370Cx50A TMS370Cx52A	SYSCLK = 0.5 MHz	See Notes 7 and 8		5	11	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				13	18	
		TMS370Cx59A†				22	28	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 10)		SYSCLK = 5 MHz,	See Notes 7 and 8		12	17	mA
			SYSCLK = 3 MHz,	See Notes 7 and 8		8	11	
			SYSCLK = 0.5 MHz,	See Notes 7 and 8		2.5	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 11)		SYSCLK = 3 MHz,	See Notes 7 and 8		6	8.6	mA
			SYSCLK = 0.5 MHz,	See Notes 7 and 8		2	3	
		Supply current (HALT mode)		XTAL2/CLKIN < 0.2 V, See Note 7			2	30

† TMS370Cx59 only operate up to 3 MHz SYSCLK

NOTES: 5. In prior versions of the TMS370 family, the I_{OL} current was equal to 2 mA for ports A, B, C, and D and the RESET pin.6. Input current I_{pp} is a maximum of 50 mA only when the EPROM is being programmed.7. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} - 0.2V.

8. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).

9. Maximum operating current for TMS370Cx50A and TMS370Cx52A = 7.6 (SYSCLK) + 7 mA. Maximum operating current for TMS370Cx53A, TMS370Cx56A, TMS370Cx58A, and TMS370Cx58B = 10 (SYSCLK) + 5.8 mA.

10. Maximum standby current for TMS370Cx5xA = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).

11. Maximum standby current for TMS370Cx5xA and TMS370Cx5xB = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit = 1, valid only up to 3 MHz of SYSCLK.)

TMS370Cx5x 8-BIT MICROCONTROLLER

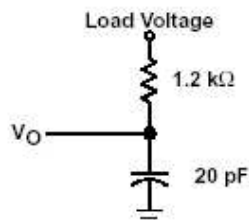
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 19. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 20. Typical Output Load Circuit (see Note A)

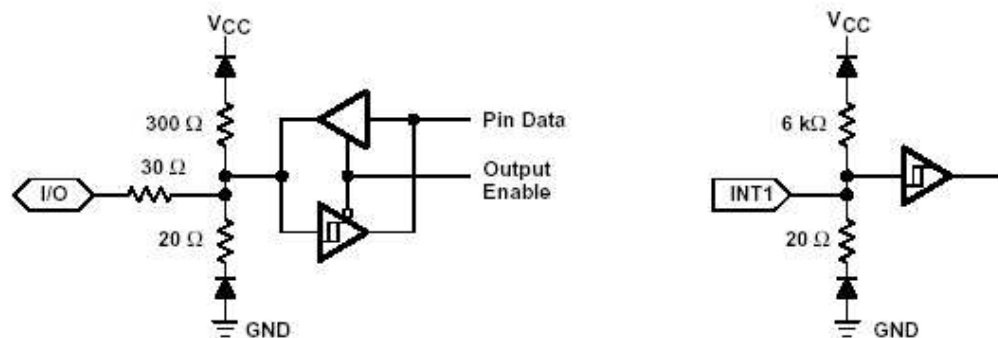


Figure 21. Typical Buffer Circuitry

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external clocking requirements for clock divided by 4[†]

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_r(CI)$ Rise time, XTAL2/CLKIN		30	ns
3	$t_f(CI)$ Fall time, XTAL2/CLKIN		30	ns
4	$t_d(CIH-SCL)$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN [‡] Crystal operating frequency	2	20	MHz
	SYSCLK [§] System clock	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.[‡] 'x59A operates up to 12 MHz CLKIN[§] 'x59A operates up to 3 MHz SYSCLK^{||} SYSCLK = CLKIN/4

NOTE 12: This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

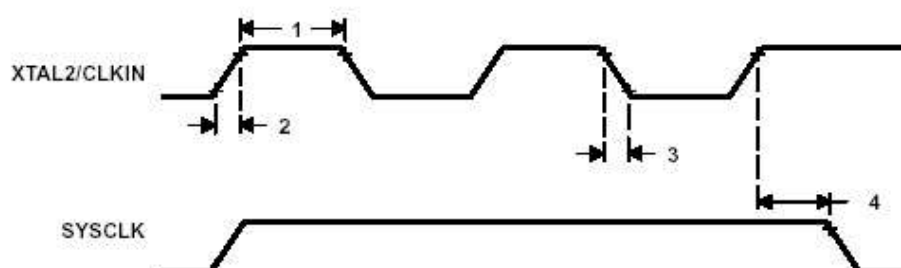


Figure 24. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)[†]

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_r(CI)$ Rise time, XTAL2/CLKIN		30	ns
3	$t_f(CI)$ Fall time, XTAL2/CLKIN		30	ns
4	$t_d(CIH-SCH)$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN [#] Crystal operating frequency	2	5	MHz
	SYSCLK System clock	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.[§] 'x59A operates up to 3 MHz SYSCLK[#] 'x59A operates up to 3 MHz CLKIN (for divide-by-1 clock option)^{||} SYSCLK = CLKIN/1

NOTE 12: This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

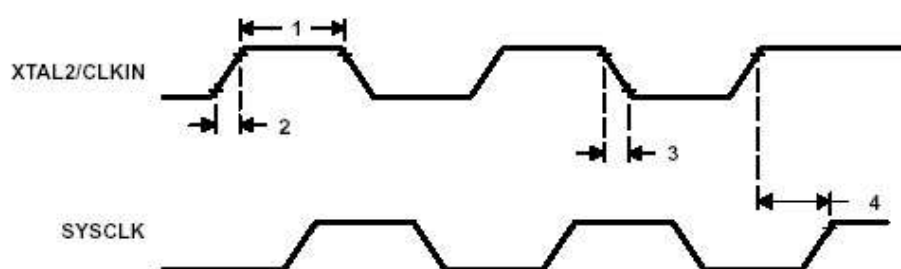


Figure 25. External Clock Timing for Divide-by-1

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general purpose output signal-switching time requirements

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

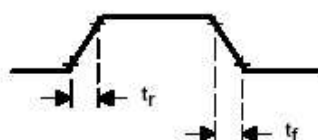


Figure 26. Signal-Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_w(\text{PGM})B$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_w(\text{PGM})AR$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC1} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13\text{ V}$)		30	50	mA
SYSCLK System clock	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_w(\text{EPGM})$ Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

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switching characteristics and timing requirements for external read and write (see Figure 27 and Figure 28)[†]

NO.	PARAMETER		MIN	MAX	UNIT	
5	t_c	Cycle time, SYSCLK (system clock)	Divide-by-4 clock	200	2000	ns
			Divide-by-1 PLL	200	500	
6	$t_w(\text{SCL})$	Pulse duration, SYSCLK low	$0.5t_c-25$	$0.5t_c$	ns	
7	$t_w(\text{SCH})$	Pulse duration, SYSCLK high	$0.5t_c$	$0.5t_c+20$	ns	
8	$t_d(\text{SCL-A})$	Delay time, SYSCLK low to address $\overline{\text{R/W}}$ and $\overline{\text{OCF}}$ valid		$0.25t_c+75$	ns	
9	$t_v(\text{A})$	Valid time, address to $\overline{\text{EDS}}$, $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, $\overline{\text{CSH3}}$, and $\overline{\text{CSPF}}$ low	$0.5t_c-90$		ns	
10	$t_{su}(\text{D})$	Setup time, write data time to $\overline{\text{EDS}}$ high	$0.75t_c-80^\ddagger$		ns	
11	$t_h(\text{EH-A})$	Hold time, address, $\overline{\text{R/W}}$ and $\overline{\text{OCF}}$ from $\overline{\text{EDS}}$, $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, $\overline{\text{CSH3}}$, and $\overline{\text{CSPF}}$ high	$0.5t_c-60$		ns	
12	$t_h(\text{EH-D}\overline{\text{W}})$	Hold time, write data time from $\overline{\text{EDS}}$ high	$0.75t_c+15$		ns	
13	$t_d(\text{DZ-EL})$	Delay time, data bus high impedance to $\overline{\text{EDS}}$ low (read cycle)	$0.25t_c-35$		ns	
14	$t_d(\text{EH-D})$	Delay time, $\overline{\text{EDS}}$ high to data bus enable (read cycle)	$1.25t_c-40$		ns	
15	$t_d(\text{EL-DV})\overline{\text{R}}$	Delay time, $\overline{\text{EDS}}$ low to read data valid		$t_c-95^\ddagger$	ns	
16	$t_h(\text{EH-D})\overline{\text{R}}$	Hold time, read time from $\overline{\text{EDS}}$ high	0		ns	
17	$t_{su}(\text{WT-SCH})$	Setup time, $\overline{\text{WAIT}}$ time to SYSCLK high	$0.25t_c+70^\S$		ns	
18	$t_h(\text{SCH-WT})$	Hold time, $\overline{\text{WAIT}}$ time from SYSCLK high	0		ns	
19	$t_d(\text{EL-WTV})$	Delay time, $\overline{\text{EDS}}$ low to $\overline{\text{WAIT}}$ valid		$0.5t_c-60$	ns	
20	t_w	Pulse duration, $\overline{\text{EDS}}$, $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, $\overline{\text{CSH3}}$, and $\overline{\text{CSPF}}$ low	$t_c-80^\ddagger$	$t_c+40^\ddagger$	ns	
21	$t_d(\text{AV-DV})\overline{\text{R}}$	Delay time, address valid to read data valid		$1.5t_c-115^\ddagger$	ns	
22	$t_d(\text{AV-WTV})$	Delay time, address valid to $\overline{\text{WAIT}}$ valid		t_c-115	ns	
23	$t_d(\text{AV-EH})$	Delay time, address valid to $\overline{\text{EDS}}$ high (end of write)	$1.5t_c-85^\ddagger$		ns	

[†] t_c = system-clock cycle time = $1/\text{SYSCLK}$

[‡] If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.

[§] If the autowait feature is enabled, the $\overline{WAIT}$ input can assume a "don't care" condition until the third cycle of the access. The $\overline{WAIT}$ signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum setup time.

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The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC1}-0.3$		$V_{CC1}+0.3$	
V_{SS3} Analog ground	$V_{SS1}-0.3$		$V_{SS1}+0.3$	V
V_{ref} Non- V_{CC3} reference†	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

† V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER			MIN	MAX	UNIT
Absolute accuracy‡			$V_{CC3} = 5.5\text{ V}$ $V_{ref} = 5.1\text{ V}$		± 1.5 LSB
Differential/integral linearity error‡§			$V_{CC3} = 5.5\text{ V}$ $V_{ref} = 5.1\text{ V}$		± 0.9 LSB
I_{CC3} Analog supply current	Converting			2	mA
	Nonconverting			5	μA
I_I	Input current, $AN0 - AN7$		$0\text{ V} \leq V_I \leq 5.5\text{ V}$		2 μA
	I_{ref} input charge current			1	mA
Z_{ref} Source impedance of V_{ref}	$\text{SYSCLK} \leq 3\text{ MHz}$			24	k Ω
	$3\text{ MHz} < \text{SYSCLK} \leq 5\text{ MHz}$			10	k Ω

‡ Absolute resolution = 20 mV. At $V_{ref} = 5\text{ V}$, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

§ Excluding quantization error of $1/2$ LSB

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The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements

	MIN	MAX	UNIT
$t_{su(S)}$ Setup time, analog to sample command	0		ns
$t_{h(AN)}$ Hold time, analog input from start of conversion	$18t_c$		ns
$t_w(S)$ Pulse duration, sample time per kilohm of source impedance [†]	1		$\mu s/k\Omega$

[†] The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

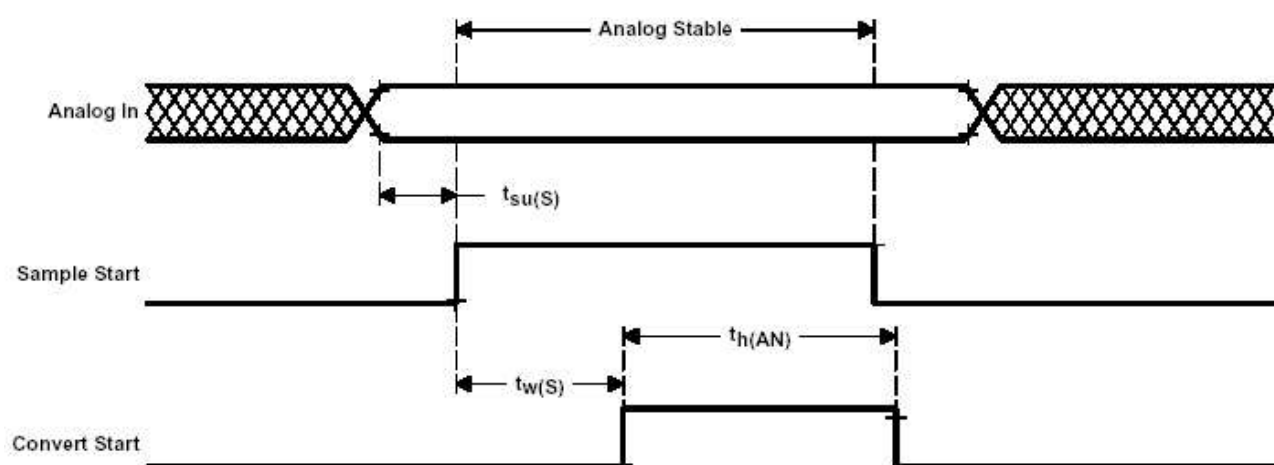


Figure 33. Analog Timing

DALLAS
 SEMICONDUCTOR

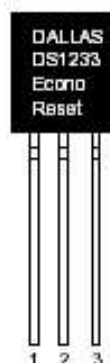
DS1233

5V EconoReset

FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5K Ω pull-up resistor
- Operating temperature of -40°C to $+85^{\circ}\text{C}$

PIN ASSIGNMENT



TO-92 PACKAGE
See Mech. Drawings
Section



SOT-223 PACKAGE
See Mech. Drawings
Section

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	RESET
PIN 3	V_{CC}
PIN 4	GROUND (SOT-223 ONLY)

DESCRIPTION

The DS1233 EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When

V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233 is pushbutton reset control. The DS1233 debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION – POWER MONITOR

The DS1233 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

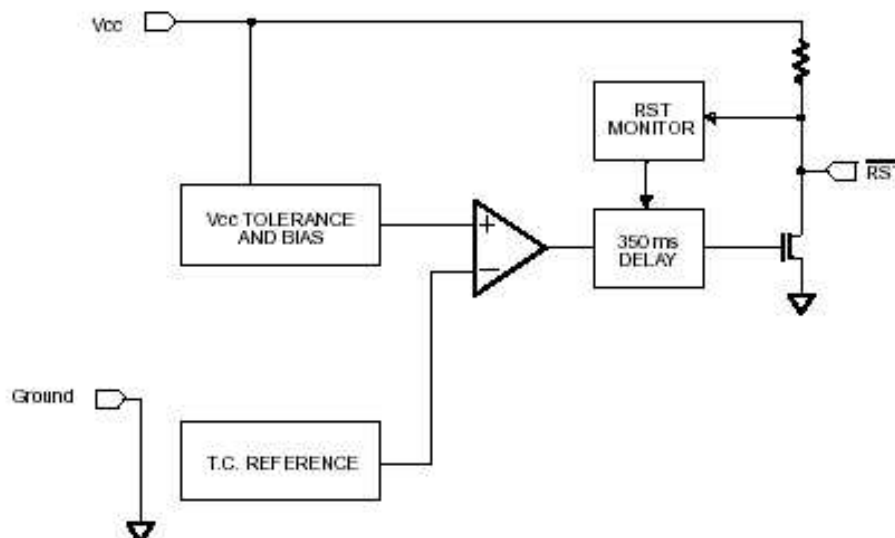
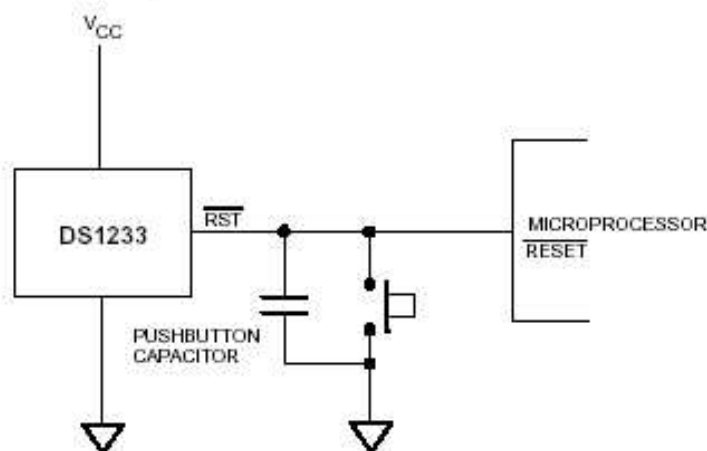
OPERATION – PUSHBUTTON RESET

The DS1233 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal

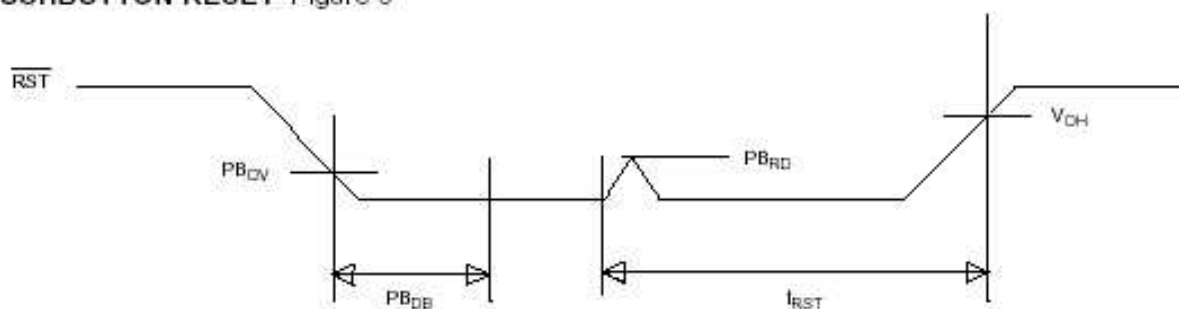
for a low going edge. If an edge is detected, the DS1233 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233 will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233 will force the $\overline{RST}$ line low and hold it low for 350 ms.

NOTE:

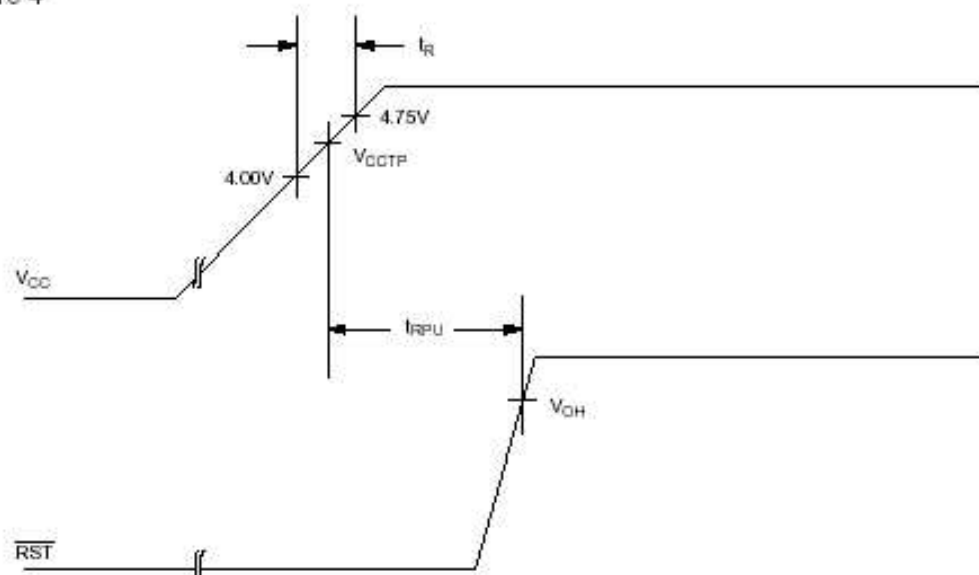
For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 μ F must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1K Ω minimum.

BLOCK DIAGRAM Figure 1**APPLICATION EXAMPLE** Figure 2

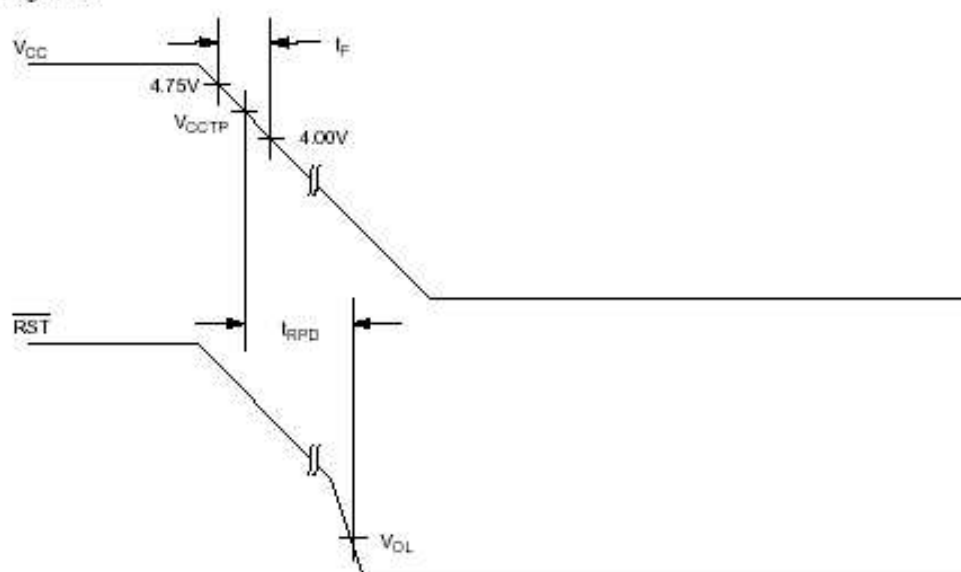
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



DS1233

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to V _{CC} +0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS(-40°C to +85°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{\text{RST}}$	V _{OL}			0.4	V	1
Output Current @ 0.4V	I _{OL}	+8			mA	
Operating Current	I _{CC}			50	μA	
V _{CC} Trip Point 5%	V _{CCTP0}	4.50	4.625	4.75	V	1
V _{CC} Trip Point 10%	V _{CCTP1}	4.25	4.375	4.49	V	1
V _{CC} Trip Point 15%	V _{CCTP2}	4.0	4.125	4.24	V	1
Output Capacitance	C _{OUT}			10	pF	
Pushbutton Detect	PB _{DV}	1.8		3.3	V	1
Pushbutton Release	PB _{RD}		0.3	0.8	V	1, 2
Internal Pull-Up Resistor	R _p	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS(-40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t _{RST}	250	350	450	ms	
V _{CC} Detect to $\overline{\text{RST}}$	t _{RPD}			100	ns	
V _{CC} Slew Rate (4.75V – 4.00V)	t _F	300			μs	
V _{CC} Slew Rate (4.00V – 4.75V)	t _R	0			ns	
Pushbutton Debounce	PB _{DB}	250	350	450	ms	
V _{CC} detect to RST	t _{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 μF capacitor connected from $\overline{\text{RST}}$ to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D-15	4.0	4.125	4.24	N/A		N/A
	DS1233D-10	4.25	4.375	4.49	N/A		N/A
	DS1233D-5	4.5	4.625	4.75	N/A		N/A
	DS1833-15	4.0	4.125	4.24	N/A		N/A
	DS1833-10	4.25	4.375	4.49	N/A		N/A
	DS1833-5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

RESISTANCE WELD THRU-HOLE CRYSTAL

HC49S

FEATURES

- Low Cost
- Stocking Standard
- Fundamental to 50 MHz (OT Temp)
- Resistance Weld
- Tolerances to < 10 PPM
- Stabilities to < 5 PPM
- Operating Temperatures to -40°C ~ +85°C
- 2.5mm Height Max (HC49SS)

OPTIONS

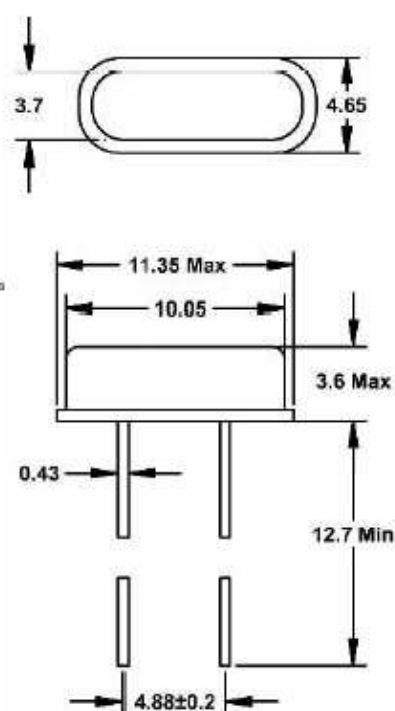


• STANDARD SPECIFICATIONS ¹	
PARAMETERS	MAX (unless otherwise noted)
Frequency Range	3.200 ~ 70.000 MHz
Frequency Tolerance @ 25°C	±50 PPM
Frequency Stability, ref @ 25°C Over Operating Temp Range	±50 PPM
Temperature Range	
Operating (T _{PR})	-20°C ~ +70°C
Storage (T _{TG})	-40°C ~ +85°C
Shunt Capacitance (C ₀)	7.0 pF
Load Capacitance (C _L)	10 pF ~ Series (Customer Specified)
Drive Level	0.5 mW
Aging per year	+5 PPM

¹Other tolerances, stabilities & operating temperature ranges available. Consult Service for specific requirements.

All specifications subject to change without notice.

Frequency Range (MHz)	Operating Mode	Max ESRW
3.200 ~ 3.500	Fundamental	300
3.500+ ~ 4.000	Fundamental	200
4.000+ ~ 5.000	Fundamental	150
5.000+ ~ 6.000	Fundamental	120
6.000+ ~ 7.000	Fundamental	100
7.000+ ~ 9.000	Fundamental	80
9.000+ ~ 13.000	Fundamental	60
13.000+ ~ 20.000	Fundamental	40
20.000+ ~ 50.000	Fundamental	30
27.000 ~ 70.000	3rd OT	100



All dimensions are in millimeters.